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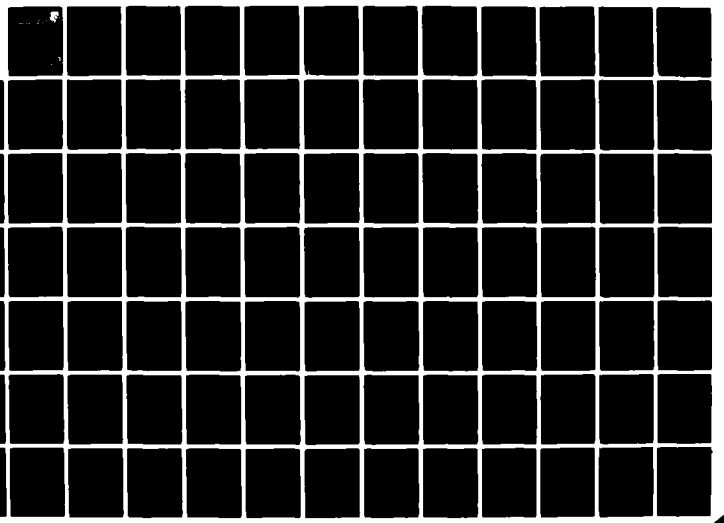

AFWAL - TR - 81 - 2128

# ADVANCED AIRCRAFT ELECTRICAL SYSTEM CONTROL TECHNOLOGY DEMONSTRATOR

## - Phase I: Analysis & Preliminary Design

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BOEING MILITARY AIRPLANE COMPANY
SEATTLE , WASHINGTON

JANUARY 1982

INTERIM REPORT FOR THE PERIOD MARCH 1981 TO OCTOBER 1981





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AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
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EMUX
Load Management
Remote Terminal (RT)
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report summarizes Task 1 and 2 and documents the results of Task 3, Phase I, of this two-phase program. Task 3 is the preliminary design of an advanced aircraft electrical system (AAES). The AAES is designed to meet the requirements of a 1990 time frame two-engine tactical aircraft with multi-mission capability. The AAES performs the functions of power generation, distribution and control of power to loads, system protection, and load management. Key characteristics of the AAES are:

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20. ABSTRACT (continued)


- Integrated avionics and power data bus configuration consisting of Digital Avionics Information System (DAIS) standard elements (MIL-STD-1750 processor, MIL-STD-1553B data bus, controls and displays, and remote terminals (RT)).
- Intelligent Electrical Load Management Centers (ELMC) capable of controlling power to loads
- Built-in-test (BIT) capability to isolate faults to the module level. BIT includes both circuit and data monitoring checks.
- Solid State Power Controllers (SSPC) to replace circuit breakers and power control switches. SSPCs are turned on/off via computer control.
- Generator control, protection and status monitoring by a Generator Control Unit (GCU) compatible with DAIS hardware and software.
- Multimission data information system through programmable system processors, ELMCs and standard DAIS elements.
- Automatic load management for increased aircraft survivability and probability of mission completion.

# PREFACE

This Interim Technical Report presents the results of work performed by the Boeing Military Airplane Company, Seattle, Washington, under Air Force Contract F33615-80-C-2004, during the period from March through September 1981. The work is sponsored by the Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, under Project 3145, Task 314529, Work Unit 31452959 with Mr. Duane G. Fox, AFWAL/POOS-2, as project engineer.

This document, which covers Task 3, Preliminary Design, of Phase I, fulfills the requirements of CDRL item number 9.

The program manager is I. S. Mehdi. The report was prepared by T. R. Boldt, G. L. Dunn, D. E. Hankins, and P. J. Leong who were technically responsible for the work.

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## SUMMARY

This interim technical report presents the results of the preliminary design of an advanced aircraft electrical system (AAES). The AAES is designed to meet the requirements for a 1990 time frame two-engine tactical aircraft with multimission capability. The system performs the following major functions on the aircraft:

- Provide electrical power to meet all mission requirements.
- Distribute electrical power to the loads.
- Provide electrical system protection.
- Control the distribution of electrical power and provide load management.

Electrical power generation consists of those functions necessary to assure that proper quality power is provided for distribution. Distribution of electrical power relates to the electrical bus structure, AC and DC, along with reliability and redundancy considerations to ensure that the generated electrical power is optimally delivered to the loads. Electrical system protection involves the automatic detection and isolation of system faults such as short circuits and generator failures. Finally, control of power distribution encompasses the on/off control of individual loads, load shedding and load sequencing.

The key characteristics of the AAES are:

- Integrated avionics and power data bus configuration consisting of Digital Avionics Information System (DAIS) standard elements (MIL-STD-1750 processor, MIL-STD-1553B data bus, controls and displays, and remote terminals (RT)).
- Intelligent Electrical Load Management Centers (ELMC) capable of controlling power to loads.

- Built-in-test (BIT) capability to isolate faults to the module level. BIT includes both circuit and data monitoring checks.

- Solid State Power Controllers (SSPC) to replace circuit breakers and power control switches. SSPCs are turned on/off via computer control.

- Generator control, protection and status monitoring by a Generator Control Unit (GCU) compatible with DAIS hardware and software.

- Multimission data information system through programmable system processors, ELMCs and standard DAIS elements.

- Automatic load management for increased aircraft survivability and probability of mission completion.

# SECTION I

# INTRODUCTION

## 1. Background

The Air Force Wright Aeronautical Laboratories (AFWAL) Aero Propulsion Laboratory has been sponsoring research and development programs directed toward applying advanced solid state power switching and computer control technology to aircraft electrical power systems. Development of components and subsystems utilizing solid state power switching and microprocessor based computer technology has progressed rapidly. Multiplexing techniques have been developed for transmission and processing of electrical system control data. This data usually consists of a large number of discrete (on/off) signals and information for solving control logic equations. Multiplex hardware and software designs have been optimized for electrical system control applications such as the B-1 E-Mux system. This, however, results in high initial development, integration and logistics costs. On large aircraft the amount of signal processing and data transfer may justify the use of a separate and optimized multiplex system for electrical system control; however, in the case of smaller aircraft this may not be the most cost effective solution.

For small aircraft, where the electrical system signal processing and data transfer may not be as large as for the B-1, it may be possible to integrate electrical system control with the avionics system in a single data bus system as developed in the DAIS program. Previous studies, such as AFAPL-TR-73-41, (Reference 1), examined this concept and concluded that integration was possible. Integration of the electrical power control was also examined in the DAIS program but was not implemented. Areas of concern with such integration are that the electrical power redundancy required for mission essential functions may not be adequate for flight critical functions. Another area of concern is that if the electrical power system is controlled by the multiplex system and in turn the multiplex system requires electrical power to operate, procedures must be devised to power-up the system. The

third area of concern is that growth of the data bus traffic may reach the point where system complexity would negate the technical and cost advantages of an integrated system.

In order to permit evaluation of aircraft electrical power system design, laboratory simulators need to be designed and built. An A-7 electrical system simulator (Reference 2) was built by the Aero Propulsion Laboratory for demonstrating functional operation of the solid state distribution concept and to show that electromagnetic interference (EMI) presented no problem. This simulator was therefore built such that it would have the same ground planes and shielding that exists on the A-7 aircraft. This type of simulator has several disadvantages such as, difficulty in maintenance due to tight hardware locations and difficulty in making changes to the wiring harness, plus poor utilization of laboratory floor space.

Modular concepts of building a laboratory simulator (Reference 3) provide the advantages of lower cost, easy modification and more universal application, even though they do not allow for adequate EMI evaluation. To date no simulator has been developed to evaluate integrated power and avionics data bus control concepts.

## 2. Program Objectives

The overall objective of this contract is to develop an aircraft electrical power distribution and control system that is integrated to the fullest practical extent with an aircraft digital avionics information management system (DAIS). Specifically this program has two distinct objectives. They are, first to define the requirements and conduct the design of a computer controlled, solid state electrical power distribution and control system for a small two engine aircraft, and second to develop the design of a laboratory simulator for evaluation of the aircraft electrical system.

## 3. Approach

To achieve the objectives of this program, a two phase study with three tasks in Phase I and two tasks in Phase II has been undertaken. The tasks for each Phase are as follows:

| | |
|---|---|
| Phase I | Analysis and Preliminary Design |
| Task 1 | Requirements Analysis |
| Task 2 | Conceptual Design |
| Task 3 | Preliminary Design |
| | |
| Phase II | Detailed Design |
| Task 1 | System Hardware and Software Design |
| Task 2 | Support Hardware and Software Design |

The program flow chart for Phase I is shown in Figure 1. During this phase, in Task 1, the requirements are defined for the electrical power system and the integrated power system control for a small two engine tactical aircraft which will be capable of performing various missions (fighter, attack, reconnaissance, trainer, electronic warfare, fighter bomber). In addition, a data base of information regarding subsystems and component hardware and software of an Advanced Electrical Power Systems (AEPS) simulator is accumulated. The requirements definition and data base is developed with the primary objective of achieving the most cost effective designs for both the aircraft electrical system and electrical system laboratory simulator. To keep the system cost at a minimum, the program is tailored so the requirements meet as closely as possible the existing electrical and DAIS system requirements and applicable hardware and software available at the AFWAL Aero Propulsion and Avionics Laboratories. Also, during Task 1 an evaluation of the Aero Propulsion and Avionics Laboratories and equipment is made. This evaluation helps to arrive at a cost effective design of the laboratory simulator through utilization of existing hardware.

In Task 2 each of 3 data bus architectures (single integrated bus, hierarchical integrated bus, separate dedicated/non-integrated bus) are configured with options ranging from all computational capability residing in the digital processor (mission computer) to most of the processing relegated to remote terminals. Based on these options, AEPS conceptual designs are prepared. A tabulation of all the relevant parameters including processor/bus loading, reliability, memory, and cost is made. The baseline for the architectural studies is the separate dedicated/non-integrated data bus. Both the hierarchical integrated bus and the single integrated bus are evaluated

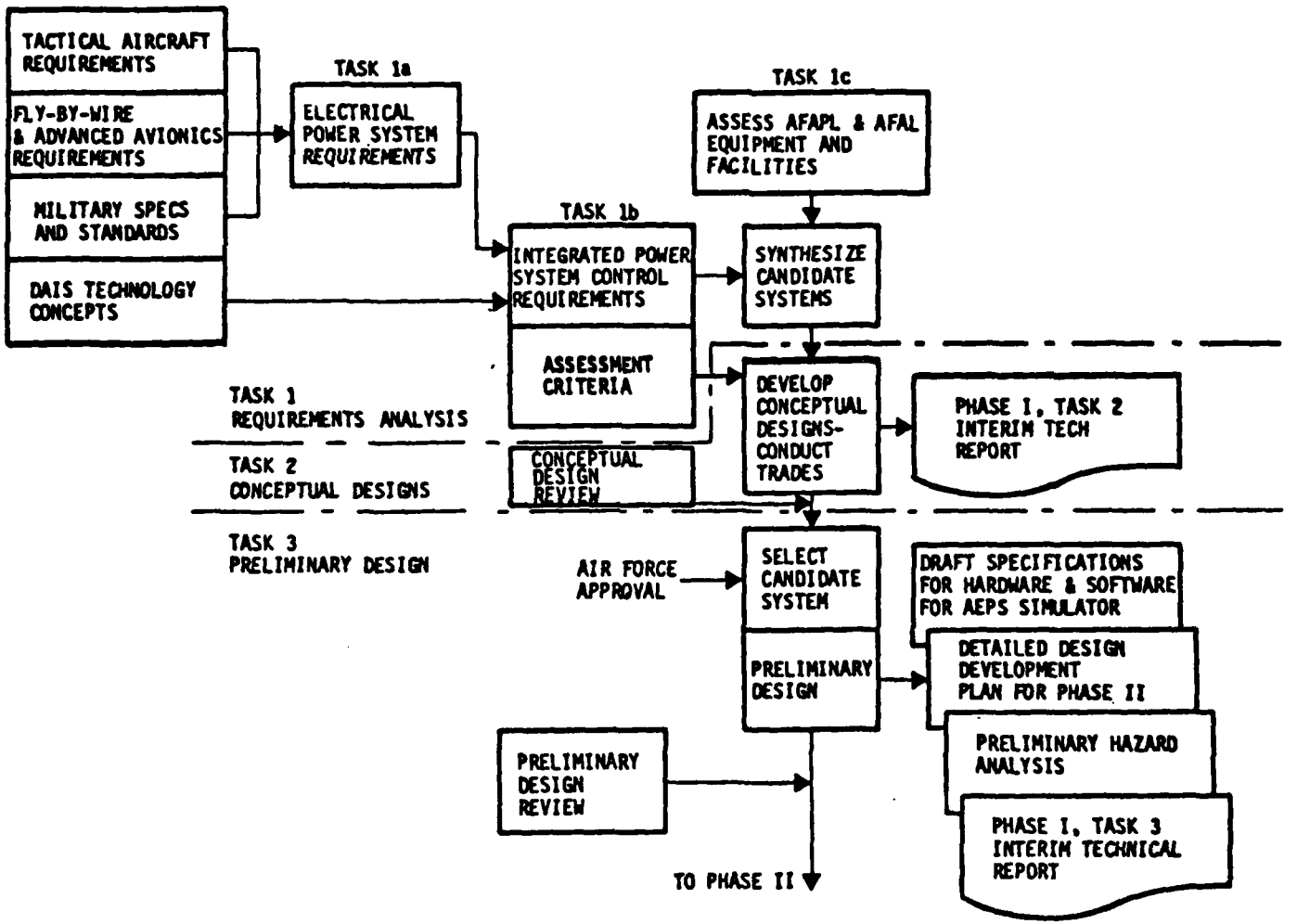



Figure 1 Phase I Program Flow Chart

against this baseline. Based on the architectural trade studies, one of the three control architectures is recommended for preliminary design.

In Task 3 a preliminary design of the electrical system with the selected architectures is conducted. System block diagrams, functional flow diagrams, data flow diagrams and key event/timing diagrams are prepared for the electrical system. Draft specifications for the hardware and software for the various components of the system are also prepared. A preliminary hazard analysis of the system is conducted and a detailed development plan for Phase II is prepared.

A report, AFWAL-TR-81-2058 (Reference 4), covering the results of Phase I, Tasks 1 and 2, has been published. This Interim Technical Report summarizes Tasks 1 and 2 and covers the results of Task 3.

## SECTION II
## REQUIREMENTS ANALYSIS AND CONCEPTUAL DESIGN

### 1. Requirements Analysis

Design options were developed for an electrical power system for a small tactical two engine aircraft with advanced avionics and fly-by-wire (FBW) flight controls. The following assumptions were made to arrive at the electrical system requirements:

- o 2 Engine Driven Generators
- o 1 Flight Operable Auxiliary Generator
- o Mission Completion With 1 Main Generator
- o Safe Return With Auxiliary Generator
- o Triple Redundant Fly-By-Wire Flight Control System
- o FBW Electronics will be Powered by DC Power
- o Solid State Distribution

A primary generator is driven by each engine. The auxiliary generator is driven by a flight operable auxiliary power unit.

The electrical power system requirements include provisions to interface with the following subsystems:

| | |
|---|---|
| Automatic Flight Control | Hydraulic Power |
| Auxiliary Power | Instruments |
| Communications | Landing Gear |
| Crew Escape | Life Support |
| Engines | Lightning |
| Environmental Control | Navigation |
| Flight Controls | Stores Management |
| Fuel | |

The degree to which each subsystem is interfaced varies. For some subsystems

such as automatic flight controls, the interface will be only to provide power and caution and warning indication. For other subsystems such as environmental control, allocations were made for more extensive interfacing, such as on/off control of equipment and sensor data communication.

a. Load Analysis

Several aircraft with different missions were surveyed with the intent of determining the effect of the mission on the generation capacity (Reference 4). The survey showed that the fighter, electronic warfare, and fighter bomber missions required the most electrical power. The power requirements were also dependent on the number of crew members.

The trend for new aircraft is toward more electrical power generation capacity. This is the result of increased sophistication in avionics, weapons, and flight control systems. Aircraft dedicated to electronic warfare missions require greater amounts of power. Next to the electronic warfare mission, the fighter and fighter bomber aircraft have the highest power requirements.

A load analysis for a two engine tactical aircraft was developed. The analysis is based on the air-to-surface fighter which Boeing is studying. The load analysis encompasses the fighter and fighter-bomber missions and also has some ECM capability. A load profile developed from the analysis is shown in Figure 2. The load analysis is summarized in Table 1.

TABLE 1. ELECTRICAL LOAD ANALYSIS SUMMARY

| | MAXIMUM CONNECTED LOAD | SUSTAINED PEAK EMERGENCY LOAD |
|---|---|---|
| TOTAL AC POWER | 58477 VA | 12577 VA |
| TOTAL DC POWER | 7805 WATTS | 2630 WATTS |
| TRU LOSSES | 1377 WATTS | 465 WATTS |
| TOTAL TRU INPUT POWER | 9182 WATTS | 3095 WATTS |
| TOTAL AC AND DC POWER | 67659 VA | 15672 VA |

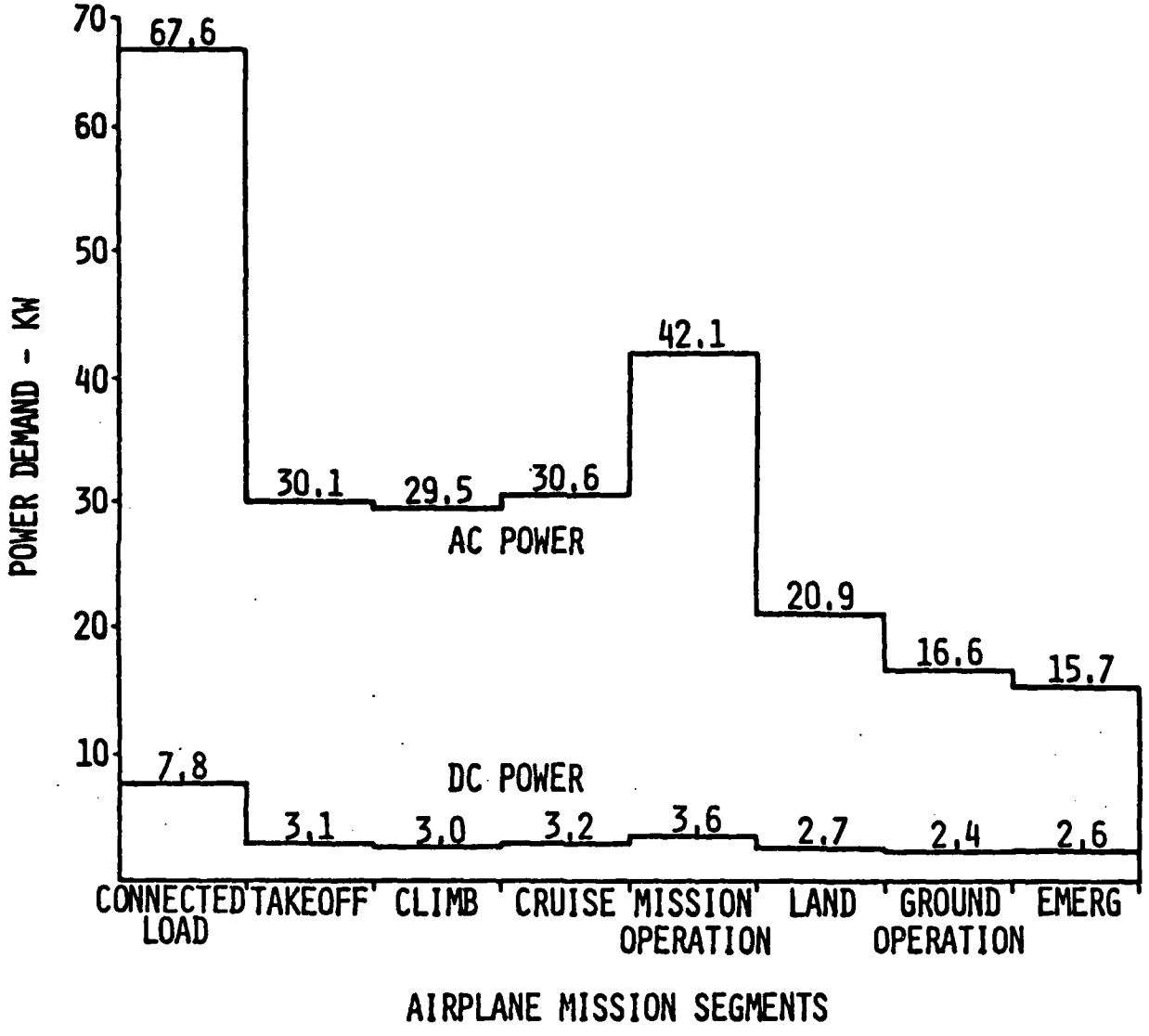



Figure 2 Electrical Load Profile

b. Generation System

Using the load analysis and the mission effects analysis as a base, the generation and distribution system was sized. The generation system complement is shown below.

2-60 KVA 115/200 VAC Generators
1-20 KVA 115/200 VAC Auxiliary Generator
3-100 Amp 28 VDC Transformer Rectifier Units

Two 60 KVA main generators allow mission completion with one generator out. Three 100 amp transformer-rectifier units (TRU) provide the system's DC power. The TRUs are sized to provide power for all connected loads. Two TRUs will provide enough DC power for mission completion.

The circuit breaker counts of three aircraft were examined. The Reference 5 study estimated about 400 solid state power controllers (SSPCs) would be required for a single aircraft. Based on the above, the number of SSPCs selected for the aircraft under study was 500. A distribution of the 500 SSPCs was also developed (Table 2). Loads requiring SSPCs larger than 7.5A AC or 20A DC will be controlled by discretely packaged SSPCs or electromechanical power controllers (EMPCs) located outside the ELMCs.

TABLE 2 SOLID STATE POWER CONTROLLER DISTRIBUTION

115 VAC

| SIZE | PERCENT TOTAL |
|---|---|
| 2A | 31.5 |
| 3A | 8.5 |
| 5A | 7 |
| 7.5A | 3 |

28 VDC

| SIZE | PERCENT TOTAL |
|---|---|
| 2A | 37 |
| 3A | 6.5 |
| 5A | 2 |
| 7.5A | 2 |
| 10A | 1.5 |
| 15A | .5 |
| 20A | .5 |

c. Distribution System

The distribution system consists of distributed load centers called ELMCs. Previous studies (References 5 and 6) have shown that this distributed concept lowers vulnerability to combat damage and in some cases lowers total system weight when compared to a single centralized distribution center. Individual loads are connected to the ELMCs rather than to the main electrical power buses as in conventional electrical systems. Power to the loads is controlled by SSPCs housed in the ELMC.

For a single engine fighter, (Reference 5) five ELMCs were recommended. The two engine tactical aircraft of this study is in the same size category. Five ELMCs provide coverage for the entire aircraft. These ELMCs would be located in the left and right forward avionics bay, left and right wing area and in the cockpit area.

The primary functions of the ELMC are to house the SSPCs and interface the SSPCs to the data bus. To maximize the utility of each box on the data bus, the ELMC will include additional functions such as those incorporated in RTs. This will minimize the number of boxes on the data bus. The additional

capabilities which will be included in the ELMCs are analog-to-digital (A/D) conversion and discrete input/output (I/O).

The ELMCs handle 15% of the system's discrete I/O data transfer. RTs handle 80% of the discrete I/O data transfer and the remaining 5% is allocated to the GCUs. Preliminary design of an RT indicates a capacity of approximately 250 inputs and 118 outputs can be packaged in a 4 MCU (1/2 ATR) size box. Based on such a design, three RTs are required to handle the I/O requirements of the system.

d. Flight Critical Power

Methods of providing power to flight critical equipment were investigated. In particular, ways of providing power to a triple redundant fly-by-wire flight control system were addressed. Two types of power are available, AC and DC. Both were evaluated for the application.

As a design philosophy, each channel of the flight control system must have its own independent power source. These sources may be cross tied for additional redundancy. For a triple redundant flight control system, three independent power sources are thus required. With DC, this provision is easily met by using three TRUs. With AC, the main generators provide two sources. A third source can be an inverter powered from a DC bus. A drawback to using AC power is the lack of a simple method for providing uninterruptible power to the flight critical equipment. With DC power, this is accomplished by diode paralleling the sources.

DC power is recommended for the flight critical systems. Two concepts were examined for providing power to flight critical equipment. In the selected concept (Figure 3), a flight critical bus is provided in the ELMC. Each bus is powered by its own TRU. Backup power is provided by a battery which is paralleled with the TRU. Any number of flight critical equipments can be connected to the bus; however, where redundancy is required, such as a triple redundant flight control system, only one channel of equipment is connected to each bus. Having a flight critical bus in the ELMC provides more versatility and reduces the number of load feeders. The vulnerability of the load due to the single feeder is minimized by short feeder lengths resulting from having 5 ELMCs distributed throughout the aircraft.

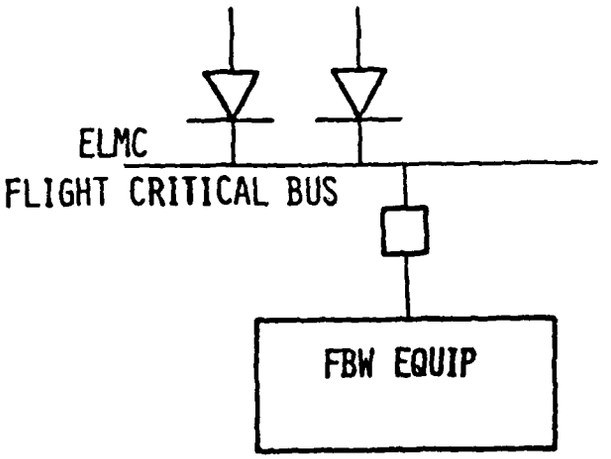



Figure 3 Flight Critical Bus in the ELMC

e. Power Bus Configuration

Two electrical power bus configurations were developed. Both configurations have provisions to support fly-by-wire flight control systems. The selected configuration is shown in Figure 4. Only three of the five ELMCs are shown.

Bus ties are incorporated in this configuration. In the AC system, the bus ties eliminate the need for separate power feeders for the auxiliary generator. The auxiliary generator supplies power to the ELMCs through the main generator buses. The DC bus ties allows the TRUs to be paralleled and to share power feeders. A disadvantage of this configuration is the additional protection required for the bus ties. Another disadvantage is the dependency of the auxiliary generator on the main generator buses for distributing power. For example, a fault on one of the two main generator buses prevents the use of the auxiliary generator if the unfaulted channel's generator is operating. This happens because the auxiliary and main generator cannot be paralleled. The simplicity of this configuration, however, translates to less wiring and, thus, less weight.

f. System Control and Protection

The system control and protection provides for automatic operation and coordinated fault isolation. Control and protection is sectionalized into the following areas: generator, distribution, and loads. The objectives of control and protection is to:

- o Reduce crew work load
- o Increase flexibility
- o Increase survivability
- o Increase probability of mission success

The reduced crew work load is achieved by automation. The use of digital processors and data bus communication lines link the various subsystems and allow coordination of most of the components of the electrical system with other aircraft subsystems.

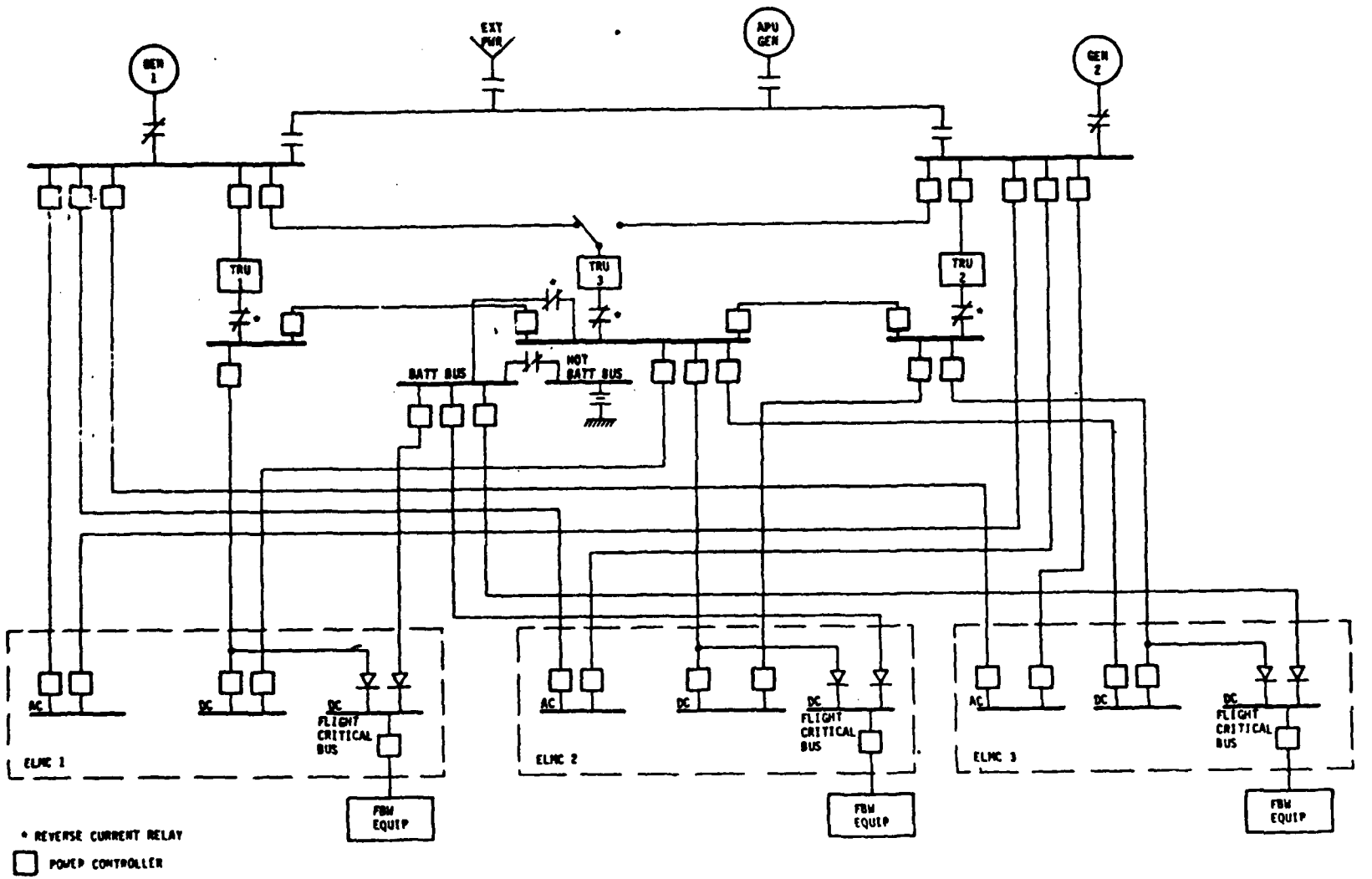



Figure 4 Power Bus Configuration

Flexibility is achieved by programmable digital processors which control the system and the individual SSPCs. The capability to reconfigure the system greatly enhances system flexibility.

Increased survivability and probability of mission success are achieved by coordination of all electrical functions and a comprehensive load management program. Automatic switching provides for fast fault isolation, bus switching, and load shedding. Load management diverts power to flight and mission essential loads in the event of a decrease in available power.

Generator control and protection functions have become fairly standardized, with only the threshold levels varying from program to program. The control and protection functions for the generator are shown below. The same functions will be applied to the APU generator.

Generator Protection

- o over/under frequency
- o open phase
- o differential protection
- o overload
- o over/under voltage
- o input underspeed
- o failed rotating rectifier

Generator Control

- o voltage regulation
- o frequency regulation
- o generator contactor

For advanced aircraft which depend on electrical power for mission completion and flight control, protection and control of the primary generating system is critical. To provide maximum fault isolation and to provide the necessary response time for the control of an aircraft generator, the control and protection of the generator is accomplished by the GCU and is not delegated to the system processors. The control and sensor lines to the generator are hardwired. The GCU is connected to the data bus. However, the generator control and protection functions operate independently of data bus service functions. This isolates the generator from data bus failures. The data bus

is used to carry data such as overload instructions, maintenance information, and fault indications, between the GCU and the system processors. Having the GCU hardwired to the generator also facilitates system startup from a "dead" airplane. In addition, loads necessary during startup are controlled by SSPCs which are in the closed state when no control signal is present.

The distribution system includes the main buses, external power receptacles and distribution feeders. The function of the distribution protection system is mainly to provide fault isolation. The protection and control functions associated with the distribution system are shown below.

Protection

- o fault protection and isolation
- o abnormal external power protection

Control

- o bus tie breaker control
- o external power breaker control
- o power distribution to ELMCs

The versatility and survivability of the aircraft is enhanced with the multiplexed data bus control of the loads. All loads are under system control and status of the loads is constantly monitored. Load control is accomplished by the solution of Boolean control equations. There is one equation for each load. The equation takes the form shown below.

$$C = \overline{L}\ P\ (R + Q)$$

C = SSPC On/Off Control Signal
L = Trip latch
P = Priority Signal
R = Request for Power (Solution of a Boolean Equation)
Q = Test Request (Such as Ground Test)

The variable R is the output of a system equation consisting of inputs from the system's RTs and ELMCs. The priority signal, P, is used to implement load management. Sixteen load management levels are available. Each level represents a different set of priority signals for the SSPCs. At each level, each SSPC will have an assigned priority, P. A P set to "0" inhibits or commands the SSPC to turn off. A "1" allows the SSPC to turn on. The relationship of the P variable and the load management levels can be visualized as a 16 x 500 matrix (500 SSPCs in the system) of "1s" and "0s". Depending on the load management level implemented, a preselected combination of 500 "1s" and "0s" are substituted for the variable P in the SSPC control equations. The load management matrix is shown in Figure 5. Various system parameters are used to logically select one of the sixteen load management levels. The level can also be selected manually. Figure 6 shows parameters which are used in determining the load management level.

g. Applicability of J73/I (JOVIAL)

The evaluation of the applicability of JOVIAL higher order language to electrical systems was investigated. A literature search aimed at a comparison of the the efficiency of assembly and higher order languages was conducted. The actual coding of two typical power control routines in both JOVIAL and assembly language was done for comparison. The analyses were performed using J73/I; however, J73/I has since been superceded by J73. The changes made in the language have been in the area of syntax and data type conversion. Also, a few new functions have been added. The differences between J73/I and J73 are minor and do not affect the results of the analyses. Based on the results of the literature search and coding evaluation, it was concluded that J73 should be used as the programming language.

h. Controls and Displays

An analysis was done to establish the requirements for the controls and displays of the electrical system. The aim of the design is to minimize the controls, and only display that information which is essential for the pilot to maintain aircraft safety and to assure mission success.

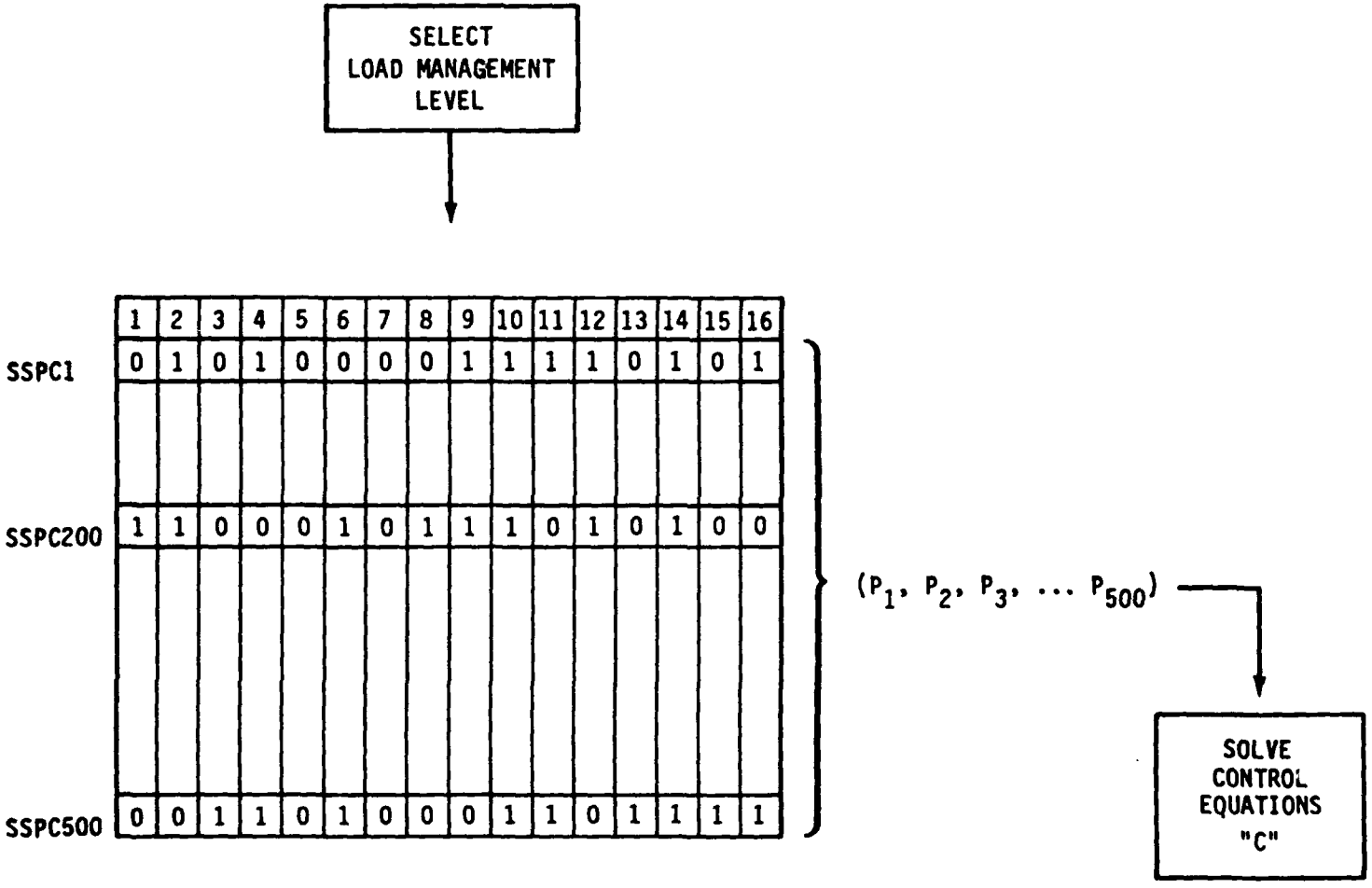



Figure 5 Load Management Matrix

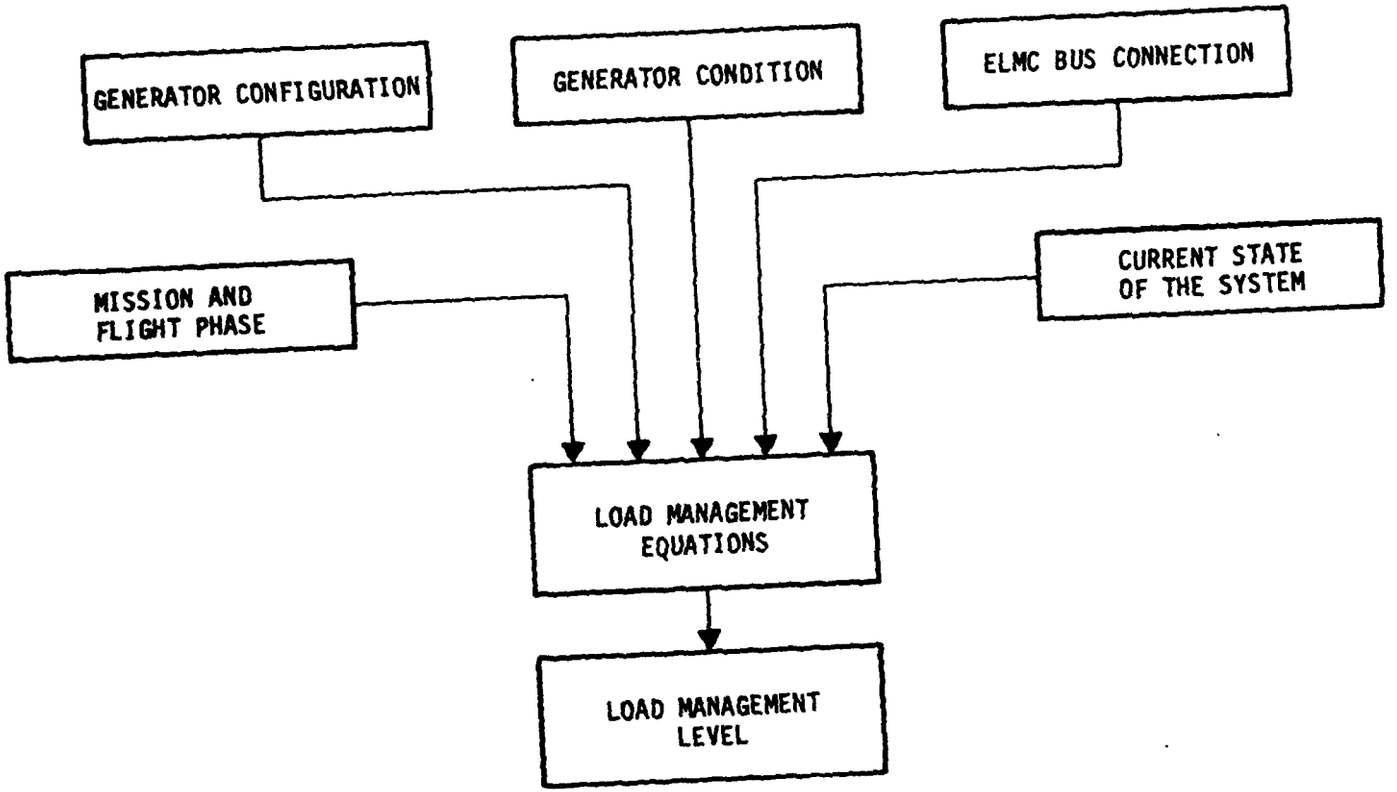



Figure 6 Load Management Level Selection

In keeping with this objective, no panel indicators are to be provided for individual SSPC status or trip indication and individual SSPC reset control. Indication of a failed or tripped SSPC appears on the appropriate subsystem warning panel or equipment warning panel. A control panel is required for the DAIS processors. It provides power to the appropriate processor during startup and restart control for any architecture.

A CRT display dedicated to the electrical system is not feasible in a two engine tactical aircraft; however, it is feasible to display electrical system data on the avionics display units. This integrated CRT display concept is possible with the integrated data bus architecture and the hierarchical data bus architecture. An example of this integrated controls/displays concept, which uses existing DAIS hardware, is shown in Figure 7. Only key system failures which affect the mission success will be displayed on the CRT.

2. Control System Requirements

Processing, bus loading, and response time requirements are defined in this section. Following are the major assumptions for defining the requirements for the integrated power system control:

a) Maximum use of Digital Avionics Information System (DAIS) concepts (Reference 7)

- MIL-STD-1553B multiplexed data bus
- RTs per specification SA 321301
- DAIS executive with synchronous bus protocol
- Use of Jovial higher order language for power system application software

b) Separate AN/AYK-15A processor for power system control.

c) Hardware connected to the 1553B bus.

- 5 ELMCs with 100 SSPCs each
- 3 Power system RTs
- 2 GCUs

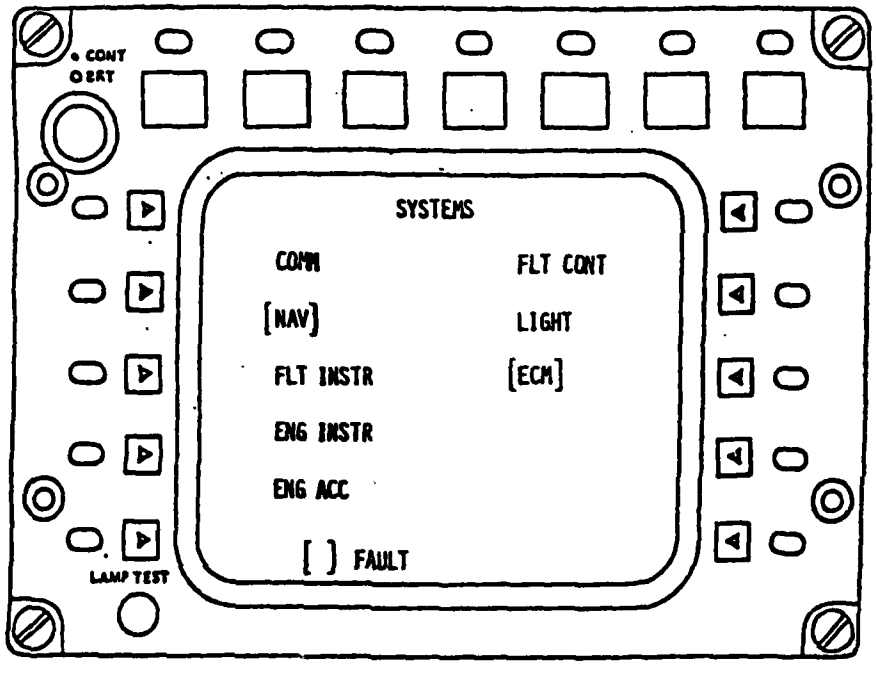



Figure 7 DAIS Integrated Controls/Displays

a. Processing Requirements

Processing requirements for the power system were based on the B-1 EMUX specification (Reference 8). Using the number of SSPCs as a complexity measure, the number and type of equations necessary for the power system in a tactical fighter was determined by scaling the equation count for the B-1 aircraft by the ratio of the SSPC\requirement for the fighter to that required in the case of the B-1 EMUX.

The processing requirements can be separated into three categories of equations as described below.

Category I: These are power request equations and are of the form Z=R where R may take one of the following forms:

| | |
|---|---|
| Form 1 | One variable of the Form A or $\bar{A}$, or the value "logic 1" |
| Form 2 | Five variables arranged in any valid Boolean expression with each variable used once only |
| Form 3 | Twenty variables arranged in any valid Boolean expression with each variable used once only |
| Form 4 | Two hundred variables arranged as the sum of products with each product term composed of no more than six variables with no variable repeated in the Boolean expression |

There will be 208 form 1, 236 form 2, 45 form 3, and 8 form 4 equations for this aircraft.

Category II: There are 500 SSPC power control equations of the form:

$$C = \overline{L}P\ (R + Q)$$

Where R is a Boolean expression of Form 1, 2, 3, or 4 listed above; P is a single variable; L is the solution to the latch equation and Q is test request.

Category III: There are 500 power system status equations of the form:

$$I = (L + PX)$$

Where L is as defined in Category II above; P and X are single variables available to the system designer for definition.

b. Input/Output Requirements

In the power system, the input/output consists of the data and traffic transmitted between the power system processor and its ELMCs and RTs in order to accomplish the power system management and control functions. The I/O requirements were determined by scaling the B-1 EMUX requirements by the ratio of the SSPC count. The discretes transmitted on the bus consist of sensor, SSPC status, system control and status, RT sync, and mode control information.

The requirements for this study were 2096 discrete inputs and 1041 discrete outputs. It was assumed that the GCU interface with the power system processor would require approximately 50 discretes for either input or output. All remaining discretes were uniformly distributed among the ELMCs and RTs. That is, each device connected to the data bus with the exception of the GCUs, contributes equally to the total discrete input and output requirements.

c. Response Time

In order to compute the processor loading and data bus loading, the response time of the system must be known. Response time refers to the maximum time required to detect a change in an event, process the information and then send a response on the data bus. A bimodal response time was used in this study. For the power system, approximately 95% of the discrete data must be received by the power system processor (PSP), processed, and the results must be transmitted within 300 ms. The remaining 5% of the equations and discrete

data must be processed for a 50 ms response time. The 50 ms response time pertains to events which require power bus switching for power distribution reconfiguration.

d. Avionics Bus Loading

The avionics bus loading is necessary so the bus loading capacity for an integrated power and avionics data bus architecture could be sized. In order to determine realistic bus loading for the avionics system, the following aircraft missions were studied: fighter, attack, reconnaissance, trainer, electronic warfare, and fighter bomber.

In order to establish a representative avionics baseline bus loading model subsystems with average complexity were selected. Data for the weapons delivery function (fire control computer, stores management, fire control radar, and laser set), inertial navigation system, and air data computer were all taken from published data for the F-16. F-16 Control and Display data was used since no fighter-bomber control and display data was available. The baseline control and display subsystem therefore consists of a fire control and navigation panel, head-up-display (HUD), and radar display. Electronic counter measures (ECM), imaging, and communications data bus loading was based on data developed at Boeing for a multi-role bomber. The ECM subsystem function is assumed to consist of flare and chaff dispersal. The imaging subsystem baseline consists of a forward looking radar.

Perturbations from the baseline in the form of incrased complexity for the control and display, inertial navigation system, ECM, and imaging subsystems for the reconnaissance, trainer, and electronic warfare missions were examined. Significant complexity increases in the inertial navigation system and the imaging subsystem exist for the reconnaissance mission. Reconnaissance missions are assumed to require a very accurate inertial navigation system and the imaging subsystem would contain side looking radar, infra-red mapping equipment, high resolution cameras, and TV cameras as well as forward looking radar. The increases in data bus loading incurred by these more complicated subsystems is expected to be neutralized by the absence of a weapons delivery capability.

In the case of the trainer a more complicated control and display subsystem is anticipated because of the requirement for dual controls and displays, and an additional monitor function for one of the pilots. The expected increase in bus traffic is estimated to be less than 20% for this subsystem.

The electronics warfare mission represents perhaps the greatest potential for increased data bus traffic from the baseline due to the large amount of data needed to identify threats and jamming as appropriate. Data from the multi-role bomber study indicates that ECM can add 8000 words/sec to bus traffic. Again this is offset by a lack of weapon delivery capability for this mission. Using the F-16 data the weapons delivery capability would add 8975 words/sec to the data bus, more than offsetting the ECM traffic.

Based on the above analysis, the number of words/sec shown in Table 3 was selected as the baseline avionics data bus loading model. The percent bus loading, based on approximately 40,000 data words/sec maximum bus loading for the MIL-STD-1553B data bus, was 36%.

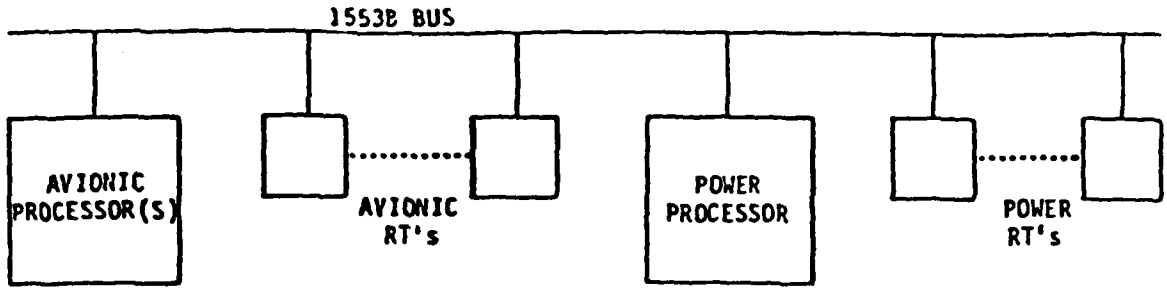
TABLE 3 BASELINE AVIONICS DATA BUS LOADING

| SUBSYSTEM | WORDS/SEC |
|---|---|
| Control and Display | 661 |
| Weapons Delivery | 8975 |
| Inertial Navigation | 3350 |
| Air Data Computer | 775 |
| Communications | 128 |
| ECM | 205 |
| Imaging Radar | 128 |
| | 14,222 |

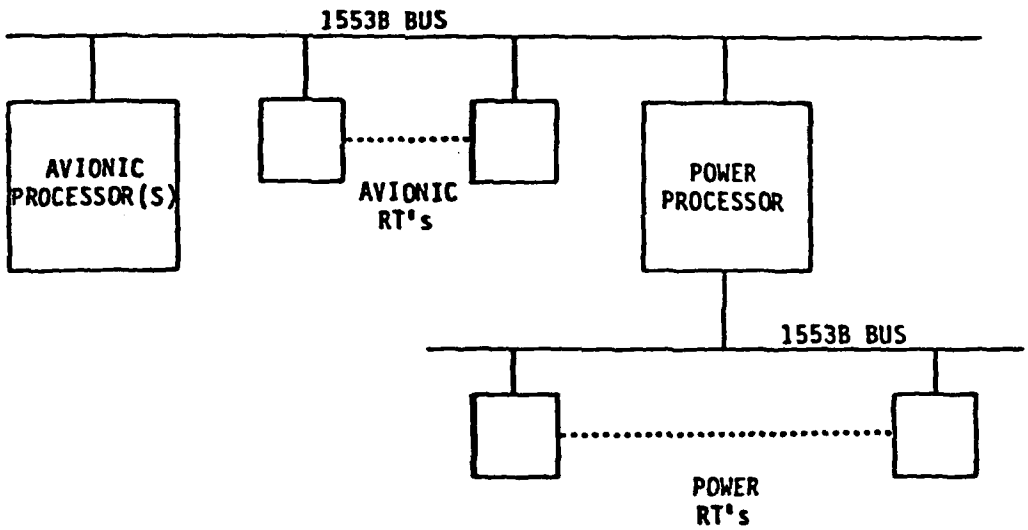
3. Technicial Analysis

A technical analysis was performed on the three separate architectures considered for electrical control. These three architectures are shown in Figure 8 and are described below:

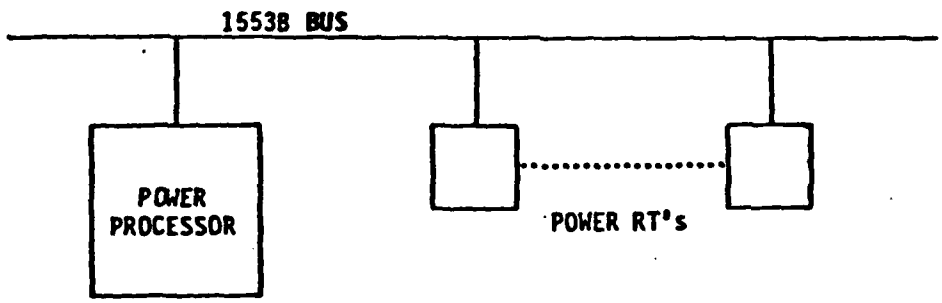
a) Integrated: The electrical control system is on the same bus as the avionics.




A: INTEGRATED ARCHITECTURE




B: HIERARCHICAL ARCHITECTURE




C: NON-INTEGRATED POWER BUS

Figure 8 Data Bus Architecture Configuration

b) Hierarchical: The electrical control system is on a separate bus but is connected to the avionic bus through an interbus processor.

c) Non-Integrated: The electrical control system is not connected to the avionic system by any multiplex data bus.

For each of these architectures the following analyses were performed:

a) Processor loading: This is calculated as the total time required to calculate the necessary set of logic equations in a minor cycle divided by the time in a minor cycle. The accepted limit for processor loading is 50%.

b) Bus Loading: This is calculated as the time required to transmit the necessary set of data, including overhead, in a minor cycle divided by the time in a minor cycle. The accepted limit for bus loading is 50%.

c) Memory Requirements: The total memory requirements for the logic equations and the executive is calculated.

d) Reliability: An architectural reliability for comparison of the integrated and hierarchical concepts is calculated.

e) Number of Processors Required: An estimate of the total number of processors is given for each architecture.

f) Smart RTs: The effect on processor loading and bus loading is analyzed using distributed processing with smart RTs.

a. General Assumptions

The analysis of the three data bus architectures was made based on the assumptions listed below. The assumptions (a) through (j) apply to all of the three architectures studied, whereas (k) through (n) apply only to the integrated data bus architecture.

a) Response time is defined to be the time required for a data change in one RT to be received by the processor, processed, and transmitted to all other RTs that require the data.

b) Bus I/O and processing are bimodal to meet separate response times of 50 msec and 300 msec. The messages that require a 50 msec response time are 5 percent of the total.

c) The system uses a MIL-STD-1553B multiplex data bus.

d) All bus transmissions are terminal-to-controller or controller-to-terminal. These are no terminal-to-terminal transmissions.

e) All bus transmissions are synchronous.

f) The system runs at 128 minor cycles per second. This provides 7.8125 msec in each minor cycle.

g) All remote terminals in the system receive the minor cycle synchronization mode code each minor cycle.

h) All data words transmitted on the bus are packed 12 data bits per 16 bit word. This will allow expansion of 4 bits per word.

i) For each architecture, there is one power system processor. This processor is a MIL-STD-1750 machine with 128 K words (16 bits each) of memory.

j) For each architecture there are ten power RTs. This includes 5 ELMCs. In the smart RT configurations, the 5 ELMCs will have a Z8002 microprocessor as the processing element.

k) The power system processor is a remote processor on the data bus. The bus controller is the avionics processor.

l) All power applications processing will occur in the power system processor. There will be no power processing in the avionics processor(s).

m) Bus loading for the avionics I/O is 36%.

n) The avionic bus controller processor will send a minor cycle synchronization mode code to the power system processor and to each of the power RTs every minor cycle. The bus time required to do this is included in the avionics bus load.

b. Processor Loading

Processor loading is defined as the amount of time within a minor cycle that the processor is busy executing application and executive code. The loading of the power system processor, smart RT with Z8002 microprocessor, and executive loading are all discussed.

Processor loading was calculated for both dumb RT and smart RT configurations. In the dumb RT configuration the power system processor calculates all equations. In the smart RT configuration the ELMC RTs calculate the category II and III equations and the processor calculates only the category I equations.

Equation calculation is bimodal to meet response time of 50 msec and 300 msec. In a dumb RT configuration, 5% of the calculations are spread over 2 minor cycles to meet the 50 msec response time and 95% of the calculations are spread over 32 minor cycles to meet the 300 msec response time. In a smart RT configuration, 5% of the calculations are spread over 2 minor cycles and 95% of the calculations are spread over 16 minor cycles.

In the smart RT configuration, each of the 5 ELMC RTs will have a Z8002 processing element. Only the processing time for the 500 SSPC complement was calculated for the smart RTs. The Category II and III equations are divided equally between the 5 smart RTs. As with power processor loading, the calculation of equations is bimodal to meet response times of 50 and 300 msec. The processing load for each RT is 21% with 5% of the processing spread over 2 minor cycles and 95% of the processing spread over 16 minor cycles.

Because each of the three architectures requires a different executive, the

processing time required by the executive is different for each architecture.

In the integrated architecture, the executive is responsible only for actions local to the power system processor. It is not responsible for bus control or system actions. In the hierarchical and non-integrated architectures, the power system processor will have an executive that is responsible for both system actions and local actions. In addition the hierarchical power processor executive will have slightly more processing requirements as a result of being a remote on the avionics bus. In relation to one another, the hierarchical executive will require the most overhead, the non-integrated executive is second and the integrated executive will require the least.

The actual percentage of processor loading during a minor cycle required by the executive is dependent on the type of executive as stated above, and on how the applications software is structured and the amount of executive services the application software requires. The more applications tasks there are, the more overhead the executive requires. A general assumption is that the executive overhead for servicing applications tasks is about 20% of the applications processor load.

c. Data Bus Loading

Data bus loading is defined as the time required to transmit the required data, including overhead, divided by the total time available. The overhead included in the bus loading analysis is inter-message gap time and message response time. Bus loading was calculated for dumb and smart RT configurations in each of the three architectures for the four different SSPC complements. The data bus I/O, like the processor loading, is bimodal to meet response times of 50 and 300 msec.

d. Memory Requirements

Estimates of memory requirements were made for the power system processor and for a smart RT. The elements that are competing for memory are listed as follows:

- o executable code for applications equations
- o other executable code for application
- o application data
- o executive code
- o executive data

The memory requirements for equation calculations can be determined exactly but only estimates can be made for the others. The memory requirement for the equations was determined by coding representative equations in the J73/I higher order language.

Other executable code for applications includes such things as control logic for the equations themselves and applications processing other than equations. The memory required for this is totally dependent on the design and structure of the applications software and cannot be accurately determined here.

Estimates can be made, however, for the memory requirements of the executive and the executive data base. The power system processor in each architecture type will require a different executive size and executive data base size. Estimates on the executive size are: 3000 words for the integrated power processor, 7000 words for the hierarchical processor and 5000 words for the non-integrated power system processor. The executive data base is dependent on the type of executive and the structure of the application software. A large number of application tasks, events, etc. results in a larger executive data base. A conservative estimate on the size of the executive data base for an average set of applications tasks is 5000 words.

e. Reliability

Reliability comparisons for the three architectures are made using the generalized reliability model. Reliability computed is not an overall system reliability. It is a computer architecture reliability and its main purpose is for comparison of the three architectural configurations.

The following assumptions were used in the reliability analysis:

a) 2.5 HR mission time for the tactical two engine airplane.
b) Processor MTBF - 3000 HRS: This MTBF was obtained from the DAIS AN/AYK-15A specification in Reference 9.
c) GCU MTBF - 4000 HRS: obtained from Reference 5.
d) ELMC MTBF - 1159 HRS
e) RT MTBF - 2354 HRS
f) Connector MTBF = $1.8 \times 10^6$ HRS

Assumptions d-f are based on Harris Corporation hardware experience.

The reliability for the respective architectures was calculated and is shown below:

Non-integrated - 0.984
Integrated - 0.976
Hierarchical - 0.976

Due to the high reliability of the connectors and since an equal number of elements are connected to the data bus for both the hierarchical and integrated architectures, the reliability is the same for these two configurations.

f. *Results of the Technical Analysis*

The major conclusions of the technical analysis performed on the three architectures are:

a) Processor loading: Smart ELMCs and an integrated architecture are necessary to meet the processing requirements for a two engine tactical aircraft.

b) Bus loading: All architectural concepts can meet the two engine tactical aircraft power system control requirements if smart ELMCs are used.

c) Memory: Smart ELMCs will require 17% more memory than the dumb ELMC configuration to meet the equation processing requirements.

d) Reliability: The hierarchical and integrated architectures have identical reliability due to the high reliability of connectors.

4. Economic Analysis

Both software and hardware costs of a two engine tactical aircraft electrical power control system architecture were examined. Software costs are for application software development only. These costs are independent of the architecture chosen. Hardware costs are relative to the baseline non-integrated architecture. Only relative hardware costs were obtained since absolute costs from the manufacturers could not be obtained for the hardware at this early stage of development. The effects of SSPC count and architectural differences were included in the analysis.

All architectural configurations studied have identical numbers of ELMCs, RTs, and GCUs. The major differences between the three concepts are in the processor reuirements.

The requirements for the power system processor for the non-integrated architecture approach can be met by the DAIS AN/AYK-15A machine both in terms of hardware and software. The requirements for the power system processor for the integrated architecture approach can also be met by the DAIS AN/AYK-15A except that the executive software will not be as extensive since here the avionics processor will have most of this responsibility. Thus, the software requirements for the integrated architecture processor will be 20% lower than that of the non-integrated architecture processor. This results in a cost reduction for the integrated architecture system over the non-integrated architecture system.

For the hierarchical architecture additional hardware and software will be required to provide the AN/AYK-15A processor with the capability to interface with two data buses and perform the interbus communications in addition to the power system processor functions. The interbus communication will result in a 40% increase in processor executive software requirements. This will, therefore, increase the cost of the hierarchical architecture processor hardware and software over the non-integrated architecture processor.

Therefore, the hierarchical architecture system will cost more than the non-integrated architecture system. From an economic standpoint the integrated data bus architecture concept is considered most appropriate for a two engine tactical aircraft.

## 5. Conceptual Design

Three power control system data bus architectures were configured using DAIS concepts to the maximum extent possible. In order to examine the feasiblity of integrating the power system control function into the DAIS architecture, two conceptural designs were configured which have varying degrees of integration with the avionics data bus. In the first design, the integrated concept, both avionics and power system control is accomplished using a common data bus. In the second design, the hierarchical concept, a separate data bus is used for the avionics and the power system control. The power system processor is connected to both the avionics and power data buses and performs the additional function of interbus processing.

The third design is the dedicated or non-integrated power system control concept. In this arrangement the avionics and power system control functions are totally separate with a separate data bus for each. Such an architecture probably could not be justified for a light tactical fighter. However, this concept was used as a baseline for comparing the two approaches described in the previous paragraph and for determining power system control requirements for a light tactical aircraft.

### a. Data Bus Architectures

All the data bus architectures presented in this section are based on the DAIS configuration. The DAIS architecture consists of federated processors communicating with each other and the other system elements (sensors, weapons, and controls and displays) through a standarized multiplex data bus. Centralized system single-point control is performed by a processor resident software executive that can be relocated for redundancy. Applications software is structured to provide modularity, reliability, and transferability. This system architecture is flexible to accommodate a wide variety

of avionics configurations, missions, and sensors, which provides redundancy to improve availability, and accommodate changes in technology.

The basic architecture is designed for a broad class of configurations where the number of processors can be reduced or enlarged depending upon the avionics and mission requirements. Standardization, modularity, and application independent executive software allows adaptability of this architecture to a broad class of different applications as well as to making mission-to-mission changes in a particular aircraft.

Sensors, weapons, and other subsystems are selected as required for the particular mission and connected to the interface modules of the remote terminals of the multiplex system or connected directly to the multiplex bus.

b. Non-Integrated Data Bus Architecture

The baseline non-integrated data bus architecture is shown in Figure 9. The configuration has two GCUs, 3 RTs, 5 ELMCs and one DAIS type processor. Power management and control software resides in this processor. In the case of a smart ELMC some of this software is moved to the ELMCs.

The major advantages of this architecture as compared to the other two candidates are:

a) simple system integration and test - due to the separation of avionics and power control functions.

b) easily expandable with minimum software impact - due to similarity with DAIS concept and existing software and hardware modularity.

c) minor changes to existing DAIS software - existing software for DAIS would be "off the shelf" and only an application software package needs to be written.

The major disadvantages of the non-integrated architecture are:

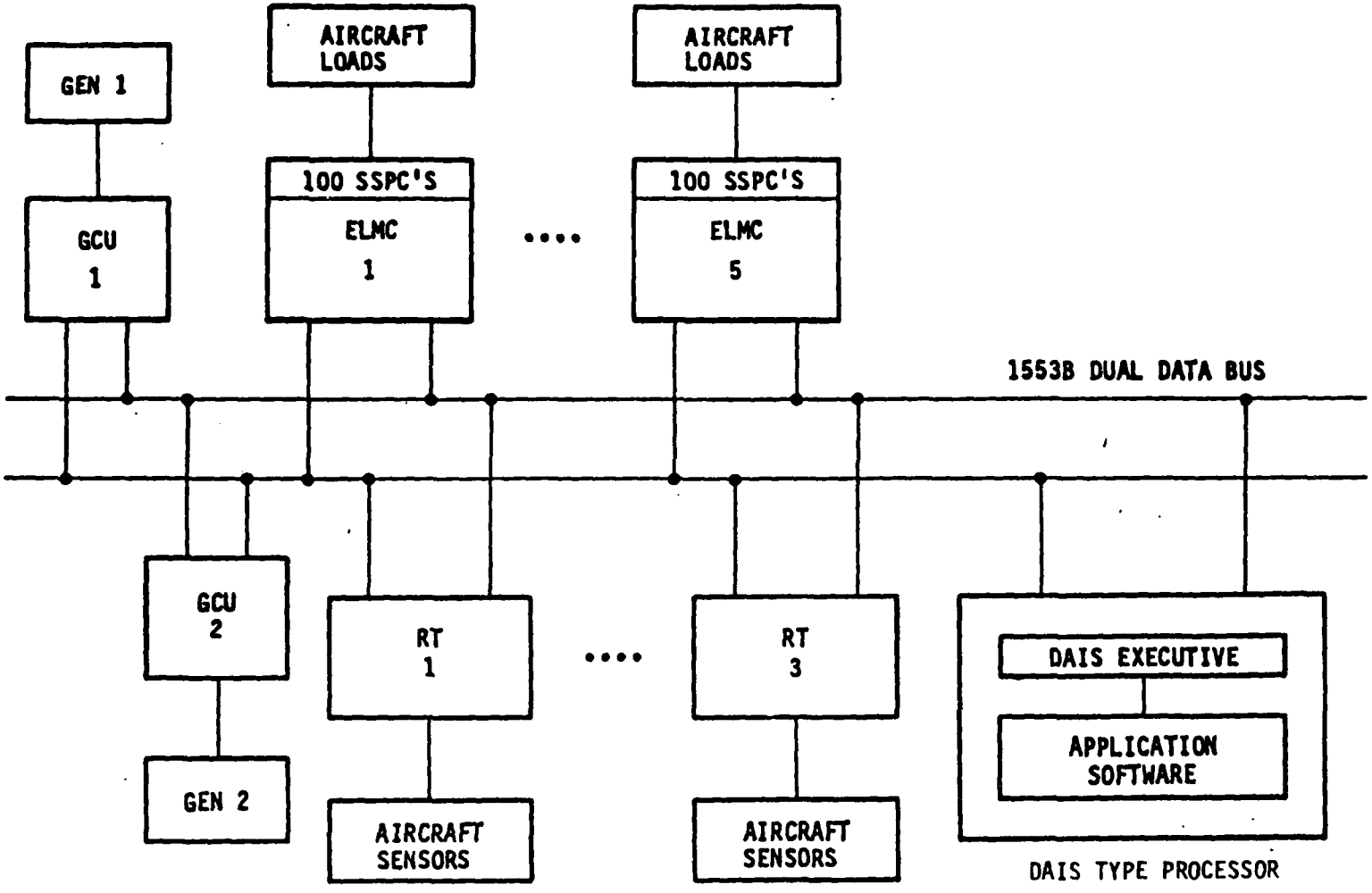



Figure 9 Baseline Non-integrated Architecture

a) redundant avionics RT interfaces - because both buses are physically separate, avionics signals needed in power system management would have to have duplicate interfaces on each data bus.

b) additional controls and displays - since there is no data path between the avionics and power control systems, multi-function controls and displays already developed for the DAIS concept could not be utilized.

c) higher bus loading - because avionics signals from the avionics bus cannot be used, these must be obtained by duplicate interfaces.

d) additional weight - due to redundant DAIS components like the controls and displays and bus interface hardware.

c. Integrated Data Bus Architecture

The integrated data bus architecture combines the avionics and power system processors on a single data bus. This concept is shown in Figure 10. The avionics processor acts as the bus controller for the entire data bus and is otherwise dedicated to avionics functions. The power system processor shares the same 1553B data bus and manages and controls its 5 ELMCs, 3 RTs, and 2 GCUs. Controls and displays are shared both by the power and avionics system. The major advantages of this concept are:

a) minor changes to existing DAIS concept - in this configuration the power system processor acts as an RT and all executive software would be "off the shelf". Only a power system application software package needs to be designed.

b) least power and weight - when compared to the other two concepts, the integrated approach minimizes the redundant use of DAIS software and hardware.

c) less memory requirements - due to the fact that the power system processor is an RT on the avionics data bus, a full executive is not necessary.

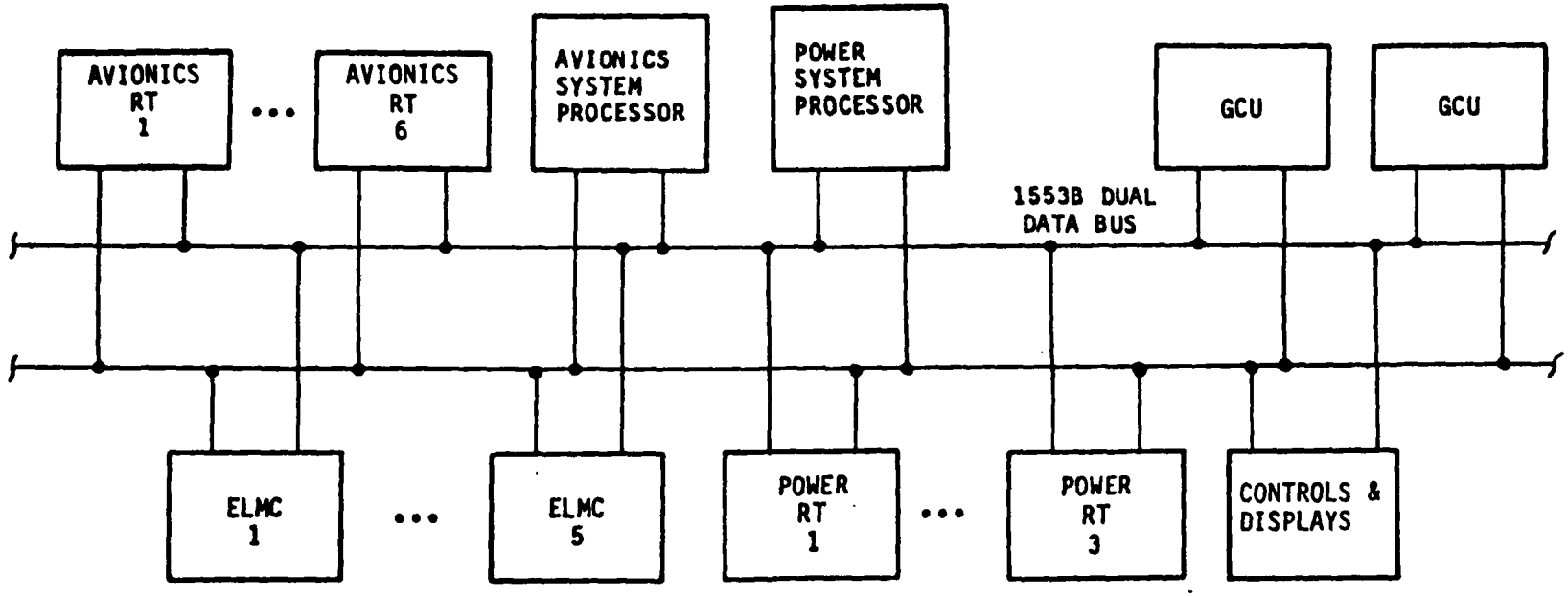



Figure 10 Integrated Architecture

The major disadvantages of the integrated concept are:

a) interaction of the power and avionics systems - changes to either system can effect the other as the bus traffic has a fixed limit of 1 megabits per second. Also response time requirements for both systems must be considered in designing data bus protocol and message handling.

b) less expandability - a single DAIS type data bus can be expanded to accommodate up to 32 elements maximum.

d. Hierarchical Data Bus Architecture

The hierarchical concept is shown in Figure 11. The key difference between this arrangement and the previous two concepts is that the power system processor is connected between a separate avionics data bus and power system data bus. The power system processor is a remote terminal on the avionics bus but a bus controller on the power system data bus. The number of RTs, ELMCs, and GCUs needed in order to accommodate the power system control requirements is the same as in previously discussed architectures. The key advantages of this approach are:

a) less bus loading - because avionics data can be obtained from a separate bus, the traffic on the power data bus is reduced.

b) greater expandability - the hierarchical data bus architecture offers almost unlimited growth potential due to the ability to cascade any number of data buses each communicating with the next via an interbus processor.

c) independence of avionics and power system - software development can progress more independently for the avionics and power system since the need to coordinate response time requirements is almost entirely eliminated.

The major disadvantages of this concept are:

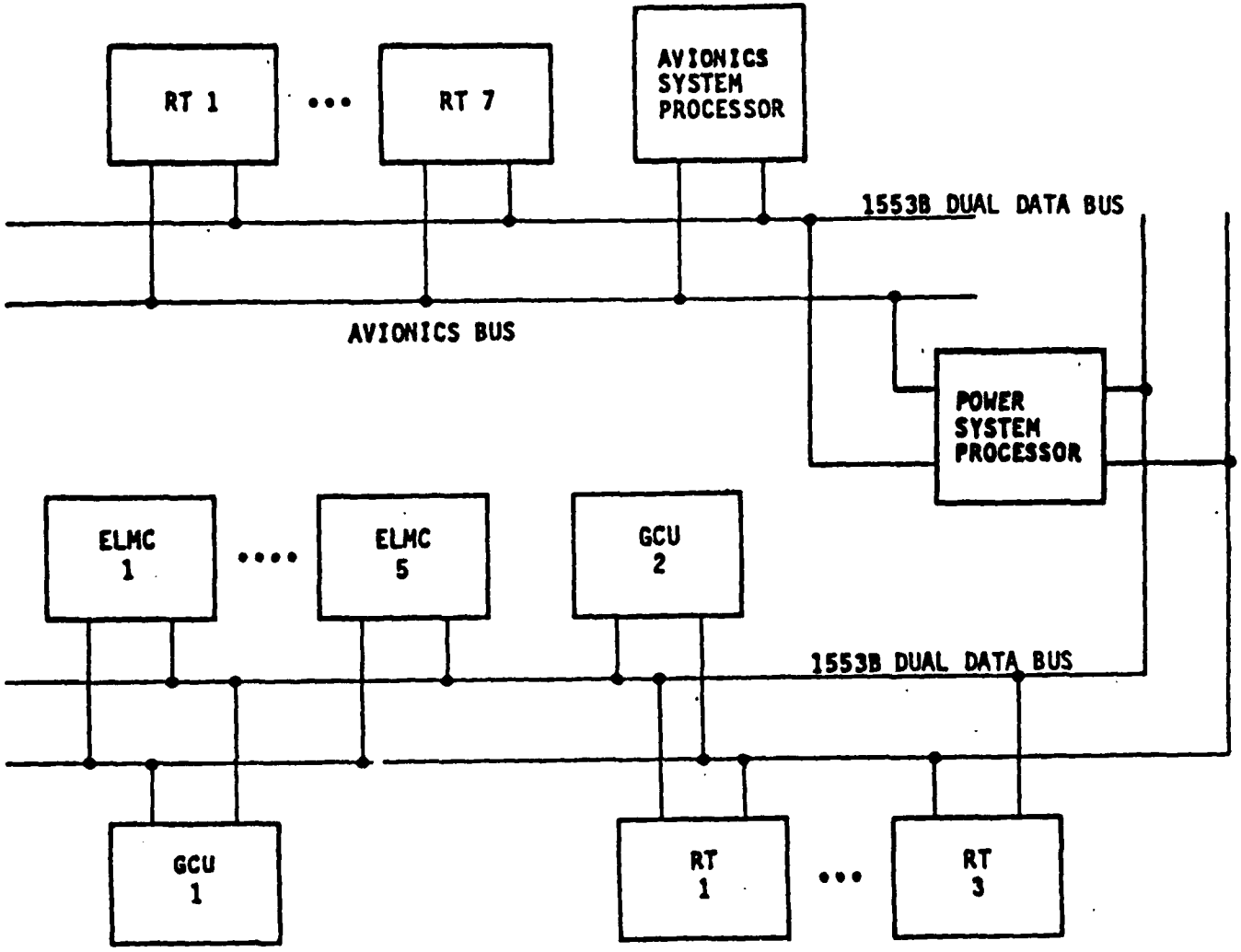



Figure 11 Hierarchical Architecture

a) immature software/hardware: both the interbus processor and its executive software for interfacing to two data buses is still in development.

b) added weight - more bus interface circuitry and power supplies will be necessary for multiple 1553B data buses than in an integrated approach.

c) higher executive overhead - a single power system processor configured to be both an RT on the avionics bus and the bus controller on the power system data bus incurs enormous software overhead.

6. Selected Concept for Preliminary Design

Based on the foregoing, an integrated avionics and power system architecture using a single data bus system was selected for the preliminary design. The system will consist of separate avionics and power system processors, 5 ELMCs, 3 RTs (for power system). The avionics processor will handle the system overhead and perform the bus controller functions. This system will manage and control an electrical system for a light tactical two-engined fighter aircraft with multimission capability.

The electrical system consists of two 60 kVA engine-driven generators, one 20 kVA auxiliary generator, three 100 A 28 VDC TRUs and 500 SSPCs. Software for this system will use the JOVAIL J73 higher order language.

The selection of the integrated architecture is based on the assumption that avionics bus loading including overhead will not exceed 36% of total capacity of a MIL-STD-1553B data bus. Also that the total number of avionics and power system elements attached to the data bus will not exceed 32.

SECTION III

ADVANCED AIRCRAFT ELECTRICAL SYSTEM PRELIMINARY DESIGN

## 1. Power System Configuration

The aircraft electrical system consists of an electrical power system and an electrical control system. The electrical system configuration is shown in Figure 12. The electrical power system consists of two primary generators which operate in the isolated mode. The two main AC buses are connected by an AC tie bus which normally is open. External power (during ground operation) and the auxiliary generator are connected to the tie bus through contactors and can provide power to both of the main AC buses. Three TRUs provide DC power to the system. One TRU is assigned to each of the two AC buses and the third TPU is powered by either AC bus. The DC system is designed to provide power to a triple redundant fly-by-wire flight control system, thus the three TRUs. A battery is used to provide emergency power and also to provide uninterruptible power to the fly-by-wire flight control system.

The electrical control system consists of a power system processor (PSP) and 5 ELMCs. Electrical power to the loads is distributed from the ELMCs. Housed in the ELMCs are solid state power controllers (SSPC) which control power to individual loads and also provide load feeder fault protection. The ELMCs also contain an imbedded electrical remote terminal (ERT) that interfaces to avionics sensors, controls the SSPCs, and provides data processing capability. Load control equations are solved in the ELMCs based on data received from the PSP. Each SSPC has a load control equation.

Three RTs are allocated to the electrical power system. These are DAIS type RTs which provide for discrete digital and analog data input and output for the system. The RTs provide the data bus interface for the system's relays and electromechanical power controllers. In addition, the RTs provide the data bus interface for the external power control unit (EPCU) and the auxiliary generator control unit (ACCU).

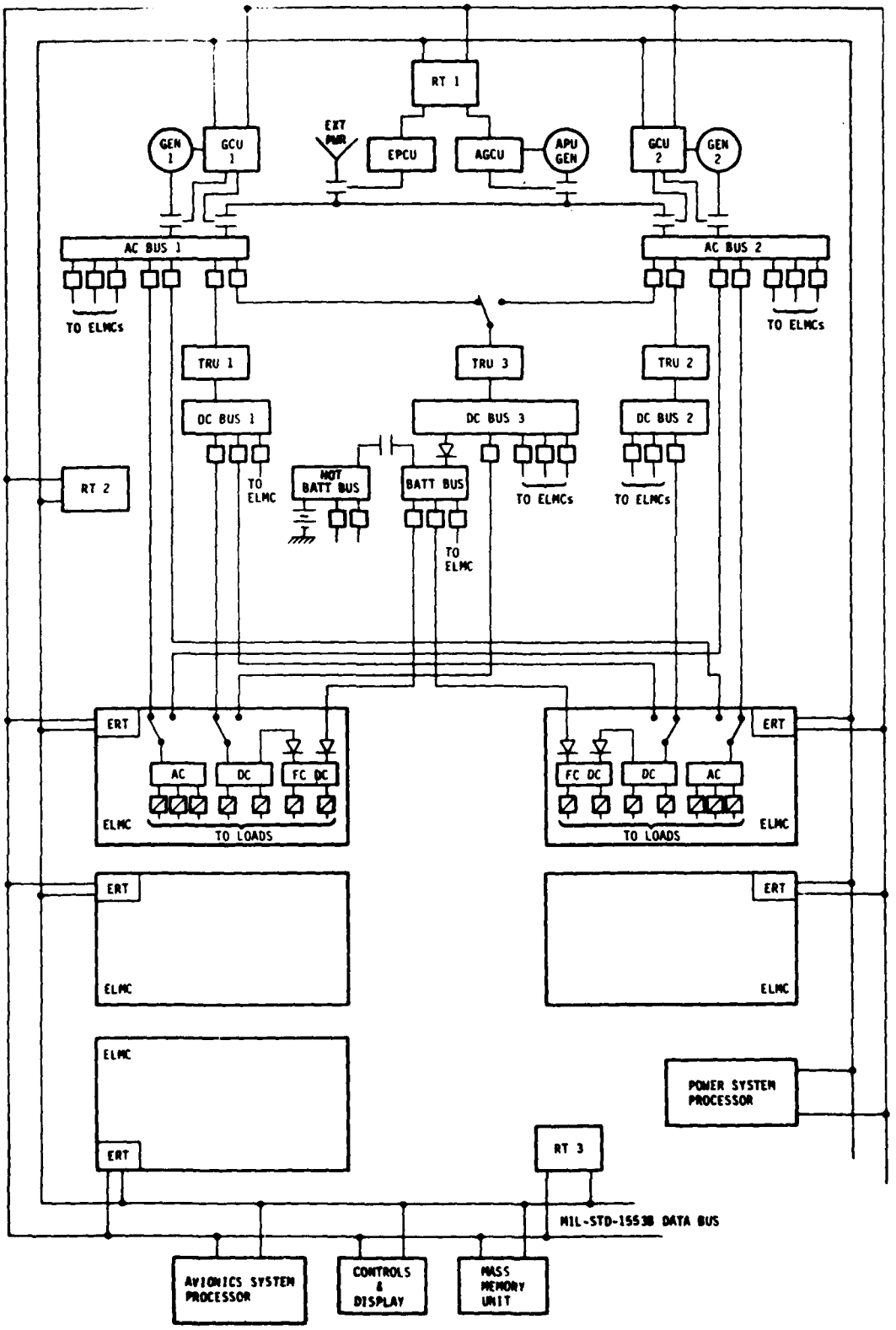



Figure 12 Aircraft Electrical System Configuration

The GCUs for the main generators provide protection and control for the generator, main AC bus, AC feeders to the ELMCs, and any loads on the main AC bus. The GCUs have a built in data bus interface unit. Generator and bus status information is sent to the PSP from the GCU. The PSP sends the GCUs a limited amount of command signals; however, the GCUs will operate independently of the bus.

The ACCU provides control and protection for the auxiliary power unit (APU) generator and control for the auxiliary power contactor. The ACCU interfaces the data bus through one of the RTs. The basic ACCU functions operate independently of the data bus. The bus is used to transmit system and generator status between the ACCU and the PSP.

The EPCU, like the ACCU, interfaces the data bus through one of the RTs. The EPCU controls the external power contactor and monitors the quality of external power.

a. System Characteristics

Primary power for the electrical power system is provided by two 60 KVA, 115/200 V, three-phase, 400 Hz generators operating isolated. 28 VDC is provided by three 100 amp transformer-rectifier units (TRU). The DC system provides the power for the flight critical equipment. A battery is provided for emergency power and for "gapless" power where the battery is diode parallelled with TRU power. AC and DC power are distributed to the loads by SSPCs contained in five ELMCs.

A flight operable APU generator is provided for emergency and ground operation. In addition, the system is designed to accept external power during ground operation.

The equipment complement list for the electrical power system is shown in Table 4. The AC and DC power system configuration is shown in Figure 13. This figure shows the distribution of power from the generators to the ELMCs. Dual redundant feeders are provided for each ELMC.

TABLE 4
ELECTRICAL SYSTEM EQUIPMENT LIST

2 - Primary Generators, 60 kVA, 115/200 V, 400 Hz
1 - APU Generator, 20 kVA, 115/200 V, 400 Hz
3 - TRUs, 100 amps, 28 VDC
1 - 24 VDC Battery
5 - ELMCs, 100 SSPCs/ELMC
3 - RTs (DAIS)
2 - GCUs (main generators) with bus interface
1 - APU GCU with RT interface
1 - EPCU with RT interface
1 - Power System Processor (DAIS)

(1) AC System

The primary AC power is provided by two 60 kVA generators. A tie bus is provided between the main generator buses. Since the generators operate isolated, the bus tie breakers (BTB) remain open during normal flight operation. The BTBs are closed during one generator operation or when external power or auxiliary power is used.

Two sets of AC power feeders are brought into each ELMC, one set from each generator bus. The ELMC selects one of the sets of feeders as a source of power for the AC loads. Both sets of AC feeders are "hot".

The AC feeders are protected by EMPCs. EMPCs are controlled by the GCUs.

The generator, the generator bus, and the AC feeder EMPCs are controlled and protected by the GCU which is described in section III.1.a.(5).

(2) DC System

The DC system is designed to provide power to a triple redundant fly-by-wire flight control system. Three 100 amp TRUs provide the DC power. A battery is

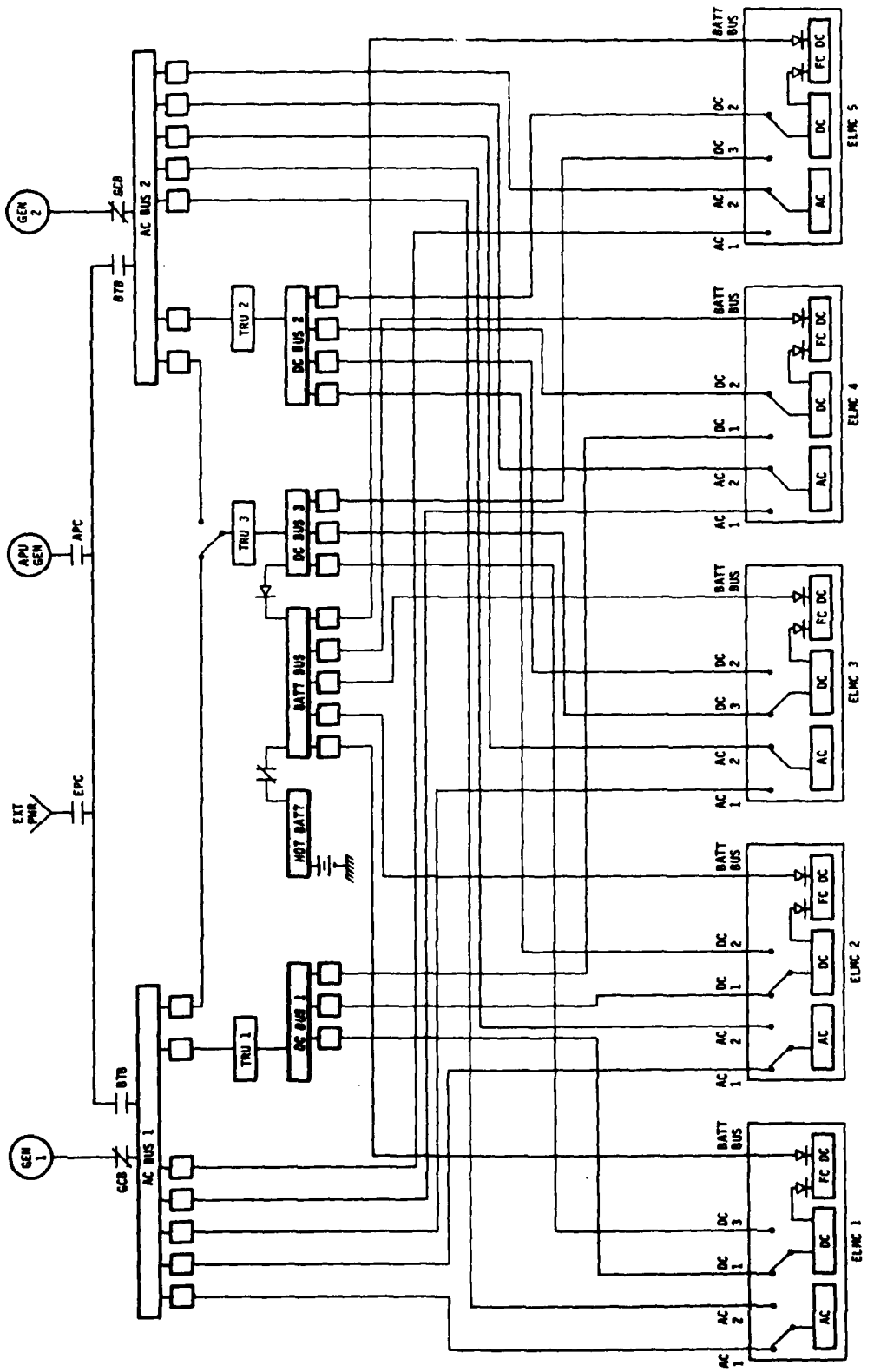



Figure 13 AC and DC Power System Configuration

used for emergency power and to provide power to the flight critical buses during bus switching.

The three TRUs are powered from the two main generator buses. One TRU is dedicated to each main generator bus. The third TRU is powered by either main generator. A relay is provided which allows the third TRU to be powered by either source. The TRU buses are isolated. With this configuration, transients occurring on a bus are isolated from the rest of the system. This represents a change from the original DC configuration shown in Figure 4.

DC power to the loads is distributed from the DC buses within the ELMCs. Each of these DC buses has two sources of power available. The ELMC central processor controls the selector relay. In the event of loss of power on the primary feeder (one feeder is designated as the primary source), the ELMC DC bus will be powered by the other feeder and source.

A battery is provided for emergency power (until the APU generator comes on line) and to provide power to the flight critical bus during bus switching outages. The battery is connected to the Hot Battery Bus. Emergency loads such as emergency cockpit lighting are powered from the Hot Battery Bus. The Hot Battery Bus is connected to the Battery Bus by a contactor which is closed in normal operation. The Battery Bus is connected to DC Bus 3 through a diode which prevents current from flowing from the Battery Bus to DC Bus 3.

The DC system provides power to the fly-by-wire flight control system. Flight critical buses in the ELMCs distribute power to the flight-by-wire equipment. The flight critical buses are powered from the DC bus in the ELMC and also from the Battery Bus. These two sources are diode parallelled. The Battery Bus provides power to the fly-by-wire equipment during power outages and during bus transfers.

(3) External Power

The system can be powered by an external AC power source. External power is applied to the AC tie bus through the external power contactor. Application

of external power to the main AC buses is controlled by the GCU through its respective BTB. The EPCU provides control and protection of the external power. From the main AC buses, the external power is distributed the same way as for aircraft power.

(4) Auxiliary Power

A flight operable APU generator provides backup power to the main generators. The APU generator is connected to the AC tie bus through the auxiliary power contactor. Control and protection for the APU generator is provided by the ACCU. Like the main generators, the APU generator operates in the isolated mode. At no time is it parallelled with any other source.

(5) Generator Control Unit

To provide the necessary response time for control of an aircraft generator, control and protection of the generator is accomplished by the GCU and is not delegated to the PSP. The GCU also provides control and protection for the main AC bus. The GCU is connected directly to the data bus; however, the generator control and protection functions operate independently of any bus service functions. This isolates the generator system from data bus failures. During system powerup, the GCUs bring the power system on line before the control system is functioning. A functional diagram of the GCU is shown in Figure 14.

Protection

An important function of the CCU is to protect the generator system from faults and to protect load equipment connected to the system from "out-of-limits" electrical power quality. The calibration and operating time delays of the various protective circuits will selectively isolate faults with a minimum reduction of generating capacity and a minimum interruption of power to airplane loads. The GCU protective functions are listed below.

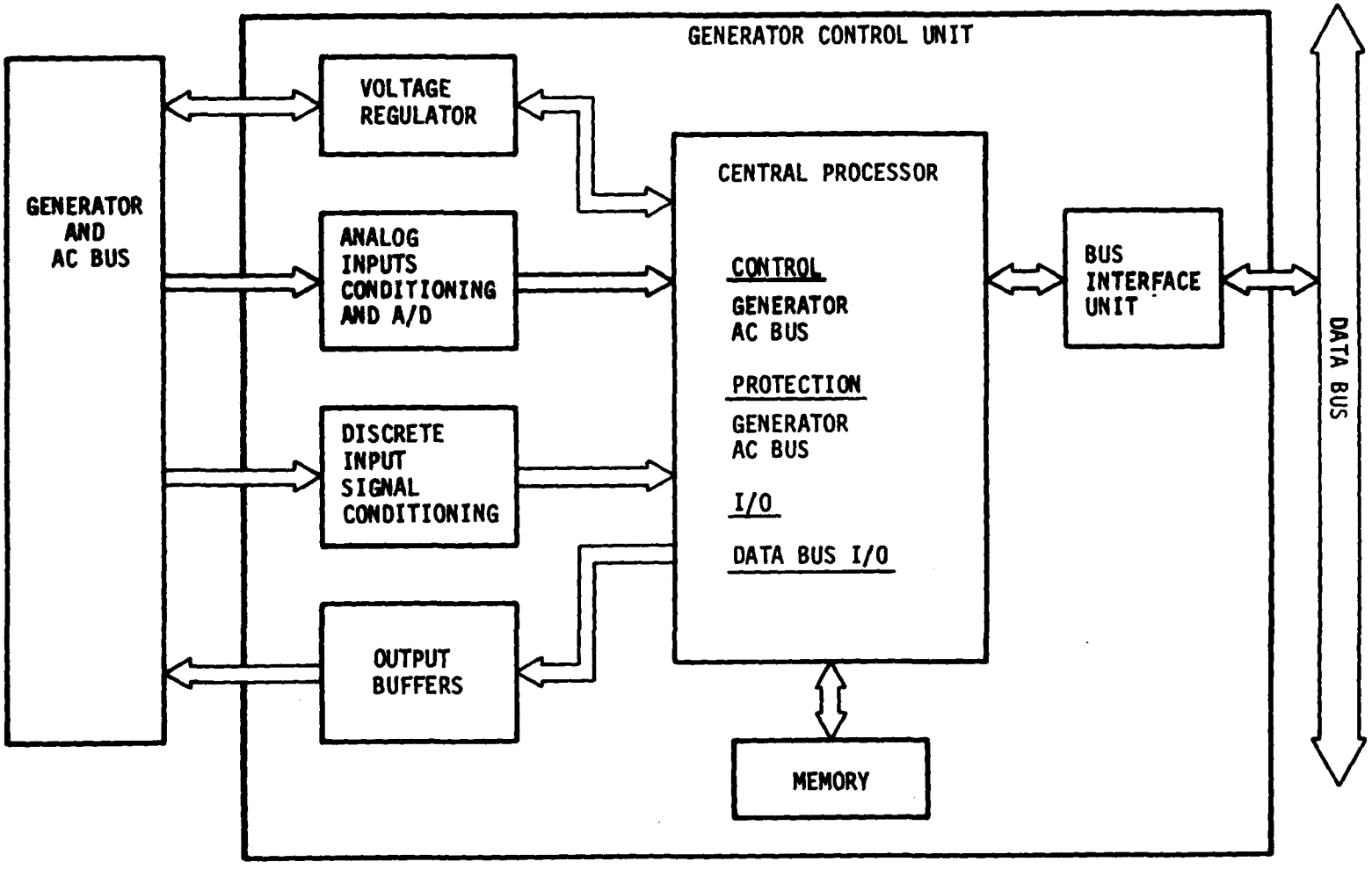



Figure 14 Generator Control Unit Functional Diagram

Function

Overvoltage
Undervoltage
Overfrequency
Underfrequency
Open Phase
Differential Fault
Failed Rotating Rectifier
Overload
Tie Bus Fault

Control

The control function of the GCU provides generator excitation and voltage regulation. In addition the GCU controls the generator circuit breaker (GCB) and the BTB.

Discrete I/O

The GCU accepts discrete input and discrete output signals for transmission to and from the PSP. In this function the GCU performs like a remote terminal. The AC ELMC feeder controllers and any load controllers on the main AC bus will interface the PSP through the GCUs discrete I/O.

b. System Operation

The electrical system is designed for automatic operation with manual override. Control of the system is distributed among the PSP, GCUs, and ELMCs.

As shown in Figure 13, each AC and DC bus in the ELMC has two sources of power. The sources are designated primary and secondary. In Figure 13, the selector relays in the ELMCs are shown in their primary positions. The selector relay for TRU 3 is also in the primary position. The system contactors are shown in their normal flight positions.

Critical to the operation of the electrical system are the GCB and BTB of each generator channel. Both are under immediate control of the GCU. The GCB will not close with the BTB closed; however, with the GCB already closed, the BTB can be closed. The GCB will close automatically when the generator power is within specified limits. The GCB will open when the power is outside these limits. If a GCB opens, the respective BTB will close and the BTB of the other channel will close. If the BTB and GCB are open and voltage is present on the tie bus, the BTB will automatically close. GCB operation will have priority over BTB operation. If the BTB is closed, it will automatically open if the GCB needs to be closed.

(1) Startup

The startup of the electrical system from a "dead" system is accomplished in two phases. In the first phase, the power generation system is brought on line. In the second phase, the control system is brought on line. Startup of the power generation system is controlled by the GCUs. When the APU generator or external power is involved in the startup process, the GCUs and the AGCU or the EPCU control the startup. The control system starts up when power is applied to the control system components (power system processor, electrical remote terminals, etc.) and the software is initialized. Figure 15 shows the startup of the complete electrical system from any one of the three sources available, main generators, auxiliary generator, or external power.

The startup of the power generation system is centered around the operation of the system contactors and relays. Figure 16 shows the operation of these contactors and relays during a system startup with the main generator. Generator 1 comes on line first, that is, engine No. 1 is started first. After engine No. 1 is started, engine No. 2 is started.

Once the power generation system has been powered up, the control system is started. The information system startup/restart function is performed with the assistance of a startup program resident in each system processor's read only memory (ROM), a system loader and the master executive.

The pilot controls the system startup/restart process via the Processor

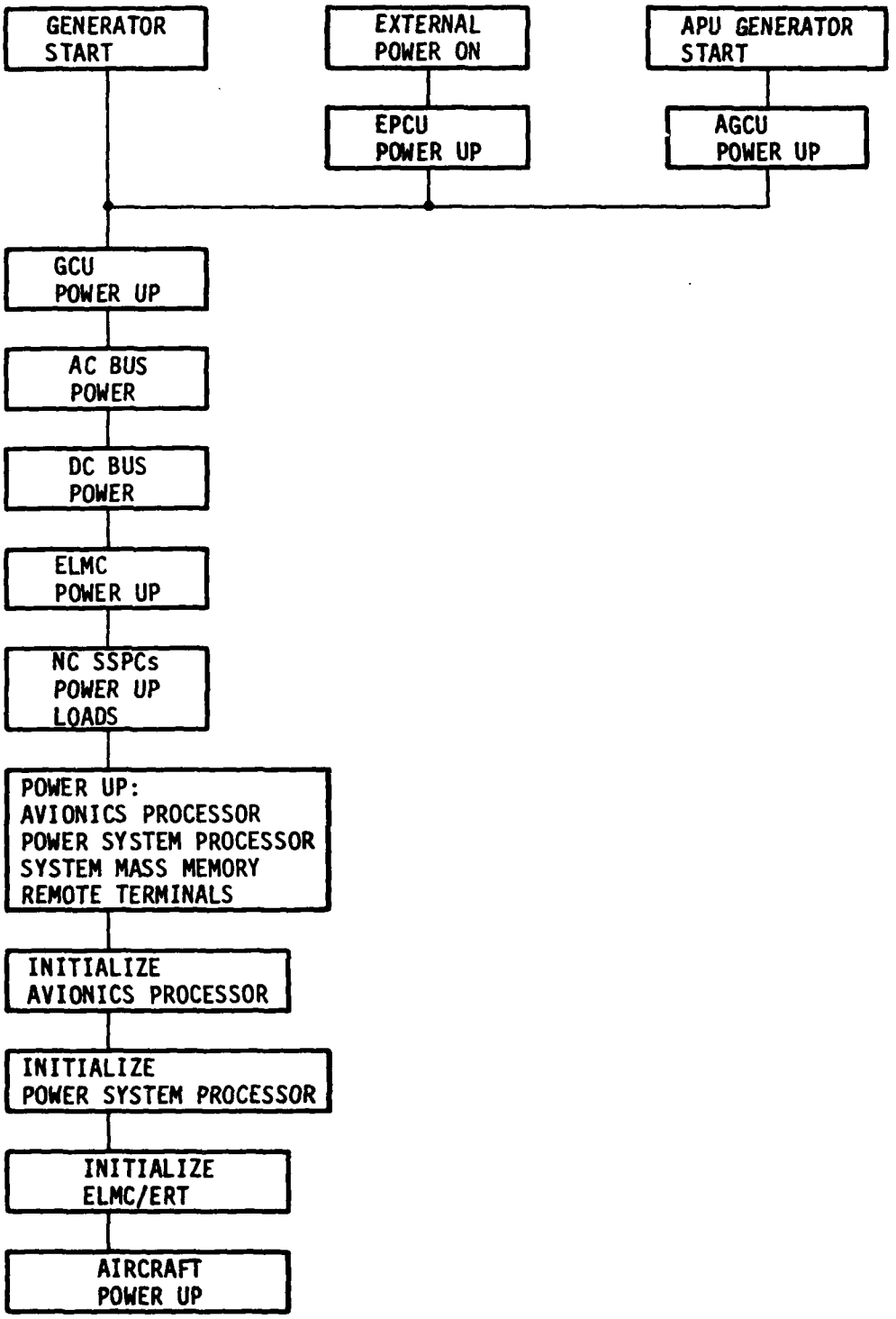



Figure 15 Electrical System Startup

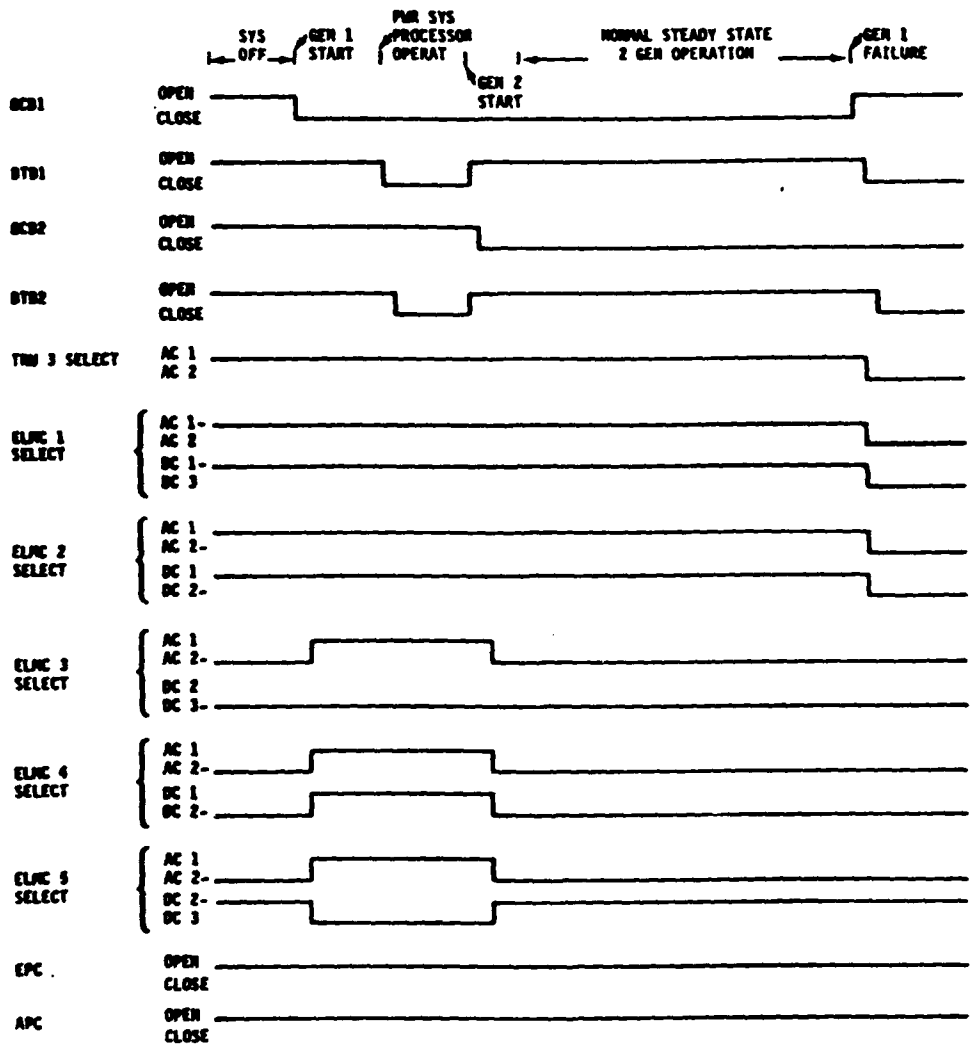



Figure 16 Power System Operational Diagram

Control Panel (PCP) as shown in Figure 17. The bus power switch allows the pilot to enable or remove power to the multiplex equipment. The processor power switches allow the pilot to enable or remove power to the processors. The GROUND position of the startup switch permits the pilot to specify initial startup as opposed to a restart, indicated by the INFLIGHT position. The start button permits the pilot to request the use of mission software already loaded, while the LOAD button allows the pilot to force the reload of all mission software.

In addition to the pilot initiated restart, the system shall perform automatic restart or system warm start. Warm start is primarily in response to a system power transient, and the objective is to get the system back up and running as quickly as possible. The procedure is to warm start the mission software in the processors and not perform a reload, if possible.

The startup/restart procedures are specified in MA 221 200 (Reference 10) and included the following functions as shown in Table 5: hardware self tests, bus control arbitration, configuration identification, mission software verification and reloading (if required), and system cold or warm start initialization.

(2) Steady State Operation

During steady state operation, the control system constantly monitors the state of the power system and the loads. Status information is fed into the system and load control equations. The solutions to the equations are transmitted to the system contactors, relays and loads. The control system gathers and processes data required to turn loads on and off.

(3) Generator Failure and Faults

System operation during a generator failure is shown in Figure 16. Generator failure operation begins under "GEN 1 FAILURE." After GCB1 trips, BTB1 automatically closes. BTB2 closes upon command from the power system processor. The ELMC and AC and DC bus selectors automatically switch to the secondary source if the primary source is affected by the loss of generator 1. Bus switching within the ELMCs, in this case, occurs independently of the PSP.

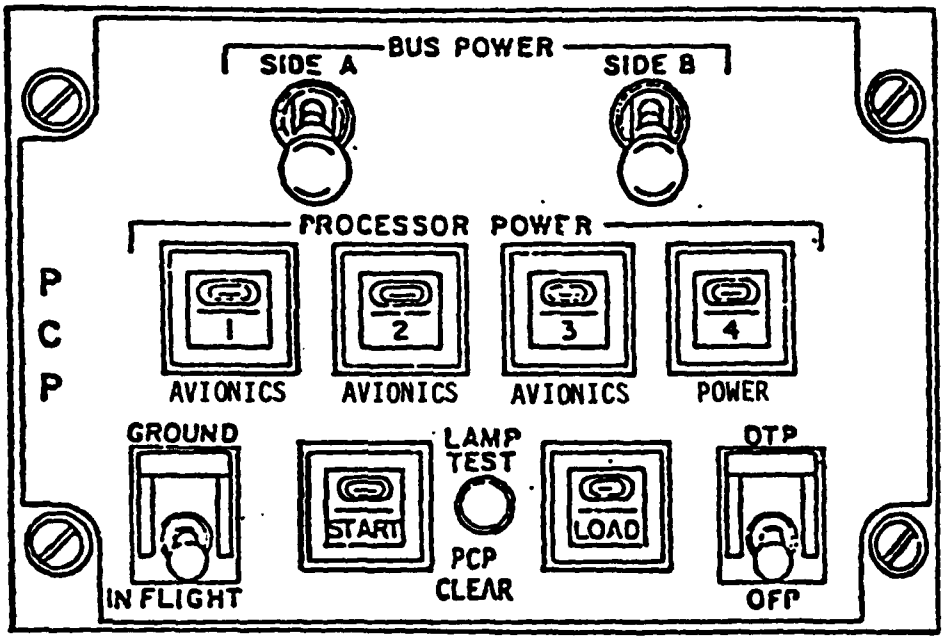



Figure 17 Processor Control Panel

TABLE 5 SYSTEM STARTUP/RESTART

| PCP SWITCH | GROUND POSITION | | | NO PCP (OR FAILED) | INFLIGHT POSITION | | |
|---|---|---|---|---|---|---|---|
| PCP BUTTON DEPRESSED | NONE | START | LOAD | | NONE | START | LOAD |
| LOAD/ RELOAD | WAIT FOR BUTTON DEPRESSION | RELOAD ONLY IF NEEDED | FORCED RELOAD | NO RELOADING | | | FORCED RELOAD |
| INITIAL-IZATION | | COLD INITIALIZATION | | WARM INITIALIZATION AS DETERMINED BY APPLICATION SOFTWARE | | | COLD INITIALIZATION |
| POWER OR PILOT INITIATED | INITIAL POWER UP- PILOT CONTROLLED | | | POWER TRANSIENT | PILOT CONTROLLED | | |

SYSTEM STARTUP

SYSTEM RESTART

All power feeders to the ELMCs are protected by EMPCs. In the event of a feeder fault, the EMPC trips the feeder off the main bus. If that feeder provided the primary power to an ELMC bus, the bus will switch to the secondary source.

(4) External Power Operation

External power is controlled by the EPCU. The EPCU closes the EPC when external power is within the specified limits. A request for external power turns off the main generator(s) or APU generator, depending on what is operating at that time, and closes the EPC and BTBs.

(5) Auxiliary Power Operation

The APU generator is controlled by the AGCU. APU generator power is applied to the tie bus through the APC. The AGCU also provides protection for the generator and controls the auxiliary power contactor. With no voltage on the tie bus, the auxiliary power contactor will close when APU generator power is within specified limits and a request for APU power is present. If the BTB(s) are open, they will close if the GCB is open. If the GCB is closed, the BTB will remain open.

(6) Processor and Data Bus Failures

In the event of a PSP or avionics system processor failure, the electrical generation portion of the system continues to function. The GCUs and the AGCU function independent of the data bus system. On/off control for the SSPCs will be lost; however, the SSPCs will remain in the same state as they were before the failure. The ERT processor will continue to operate, performing the ELMC power bus switching functions when necessary.

(7) Load Management

Load management is divided into the areas of bus switching and load shedding. Following is a description of each of these areas for the AAES.

Bus Switching

The AAES allows for redundant power paths for both AC and DC power. Bus switching as defined in this section relates to the switching of redundant power distribution lines which exist between the main AC and DC buses and the buses located in the ELMCs. Control for bus switching resides in two locations, the ELMCs and the power system processor.

Load Shedding

Load management is achieved through load management routines which are included as an integral part of the AAES system software. Sixteen levels of management are available. Each management level allows three possible variations of the power control equation. The equation may be (1) solved normally, ((2) have its solution forced to "0" or (3) have its solution forced to "1". This in effect allows the equation itself to be modified at each management level.

2. Integrated Power System Control

A single integrated data bus system is used to control the electrical power system. The integrated architecture combines the avionics and power system processors on a single data bus. A functional diagram of this concept is shown in Figure 18. The avionics processor acts as the bus controller for the entire data bus and is otherwise dedicated to avionics functions. The PSP shares the same 1553B data bus and manages and controls its five ELMCs, three RTs, and two CCUs. Controls and displays are shared both by the electrical and avionics systems.

a. Multiplex Data Bus Characteristics

The multiplex data bus used in the integrated avionics and power information system conforms to MIL-STD-1553B requirements. Following is a brief description of the key requirements of this standard. The bus operates at a maximum data rate of 1 megabits/sec. The data transferred over the bus is coded as Manchester II bi-phase levels. Data words are 16 bits plus the sync

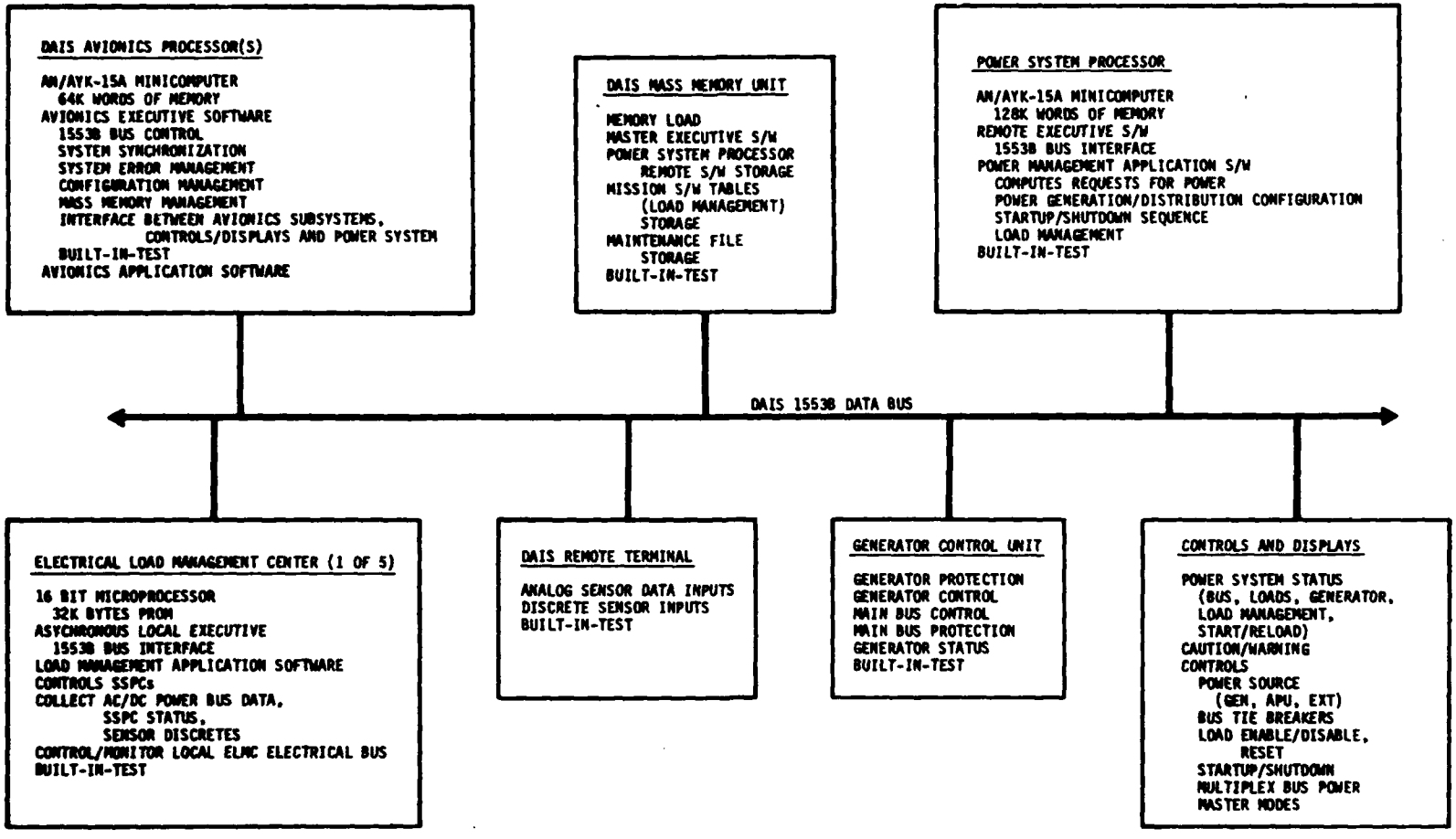



Figure 18 Integrated Avionics and Electrical Control System Functional Diagram

waveform and the parity bit for a total of 20 bit times as shown in Figure 19. Also, as shown in Figure 19, word formats consist of three types: command, data, and status.

Sole control of information transmission on the bus resides with the bus controller, which initiates all transmissions. Command words sent by the bus controller to devices connected directly to the 1553B data bus contain an optional mode code field as shown in Figure 20. These mode codes are shown in Table 6 and are used by the RT to control information flow.

The command, data, and status words defined above are grouped to form messages for transmission over the data bus. Allowable message formats are shown in Figure 20. No other message formats are permitted.

b. Avionics/Electrical Control System Interface

The multiplex data bus provides the interface between the avionics system and the electrical control system. The avionics processor controls the data bus and as a result, provides overall system synchronization and timing.

Information exchanged between the avionics system and the electrical control system includes electrical system startup and shutdown commands issued by the avionics processor, controls and displays data, and avionics sensor data. Data that is received from aircraft controls is first interpreted by the avionics system, and if this data requires processing by the electrical control system, it is transmitted to the power system processor. Similarly, electrical control system data that needs to be placed on aircraft displays is sent to the avionics processor by the power system processor. Finally, ERTs in the electrical control system may, as part of their function, interface to avionics sensors. Data collected from these sensors is transmitted directly to the avionics processor.

c. Electrical Control System

The electrical control system consists of a distributed network of processors, controllers, and terminals that monitor the electrical power system and exert

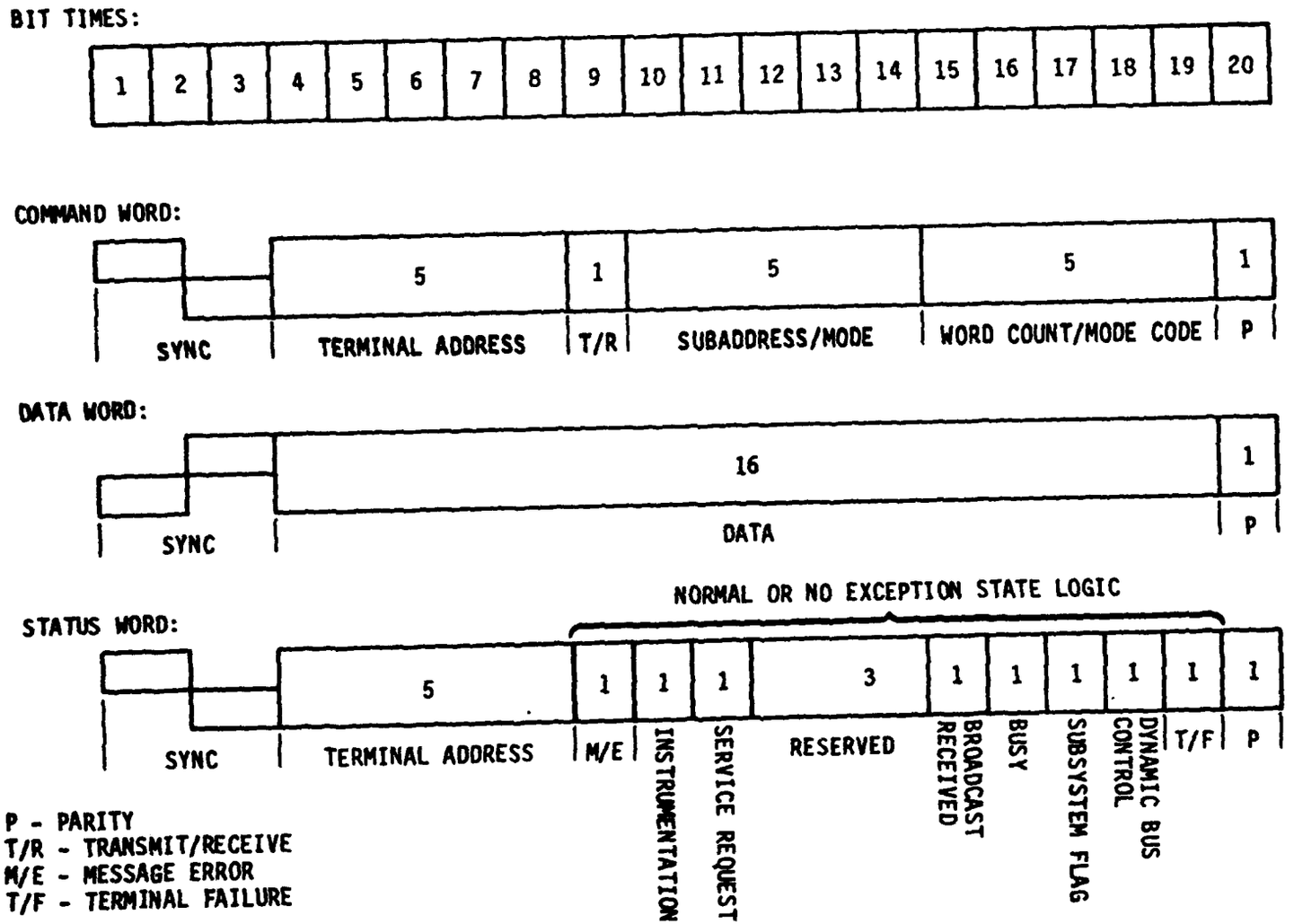



Figure 19 15538 Bus Message Word Formats

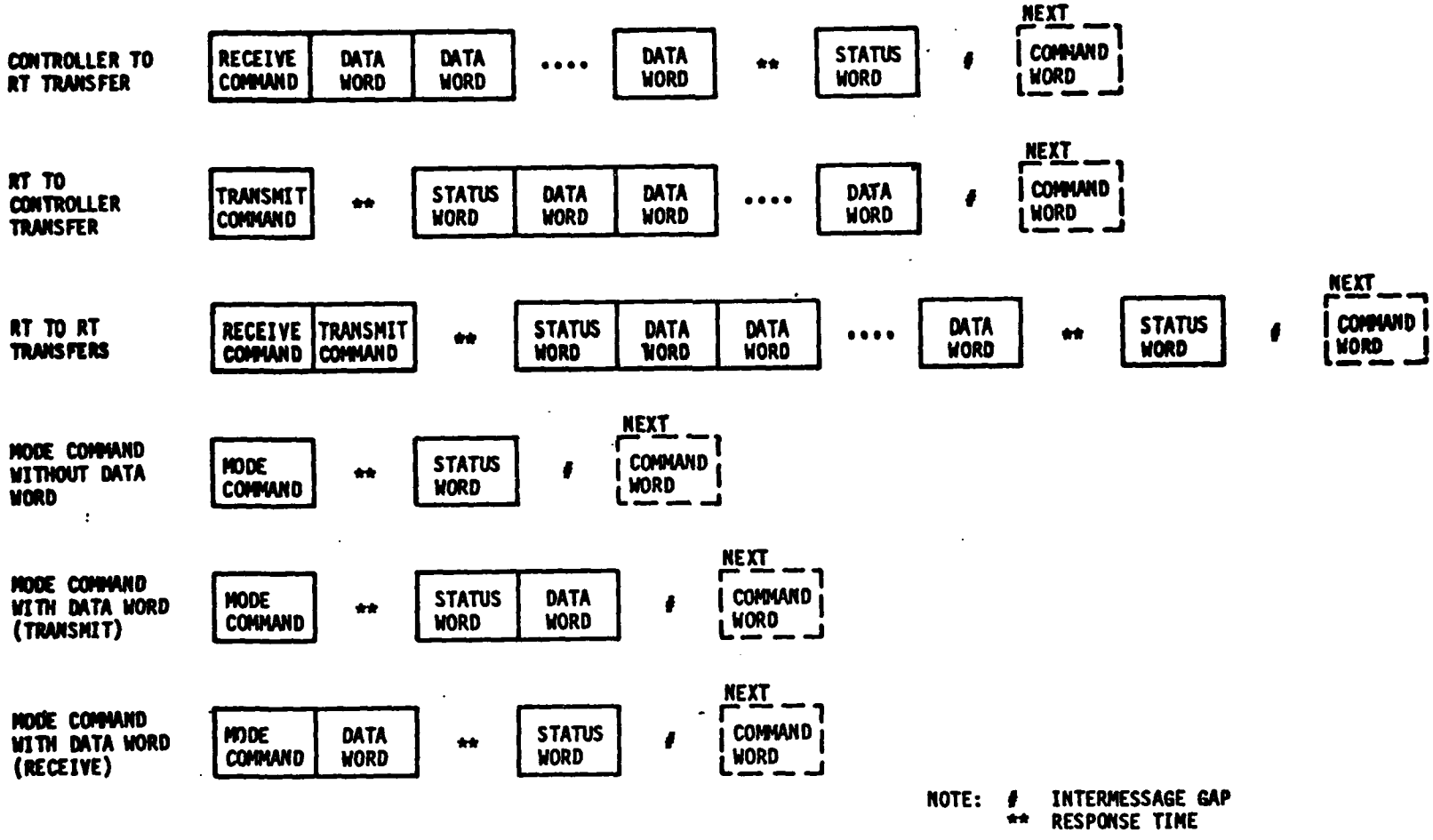



Figure 20 Bus Message Formats

TABLE 6 BUS MESSAGE MODE CODES

| T/R Bit | Mode Code | Function | Associated Data Word | Broadcast Command Allowed |
|---|---|---|---|---|
| 1 | 00000 | Dynamic Bus Control | No | No |
| 1 | 00001 | Synchronize | No | Yes |
| 1 | 00010 | Transmit Status Word | No | No |
| 1 | 00011 | Initiate Self Test | No | Yes |
| 1 | 00100 | Transmitter Shutdown | No | Yes |
| 1 | 00101 | Override Transmitter Shutdown | No | Yes |
| 1 | 00110 | Inhibit Terminal Flag Bit | No | Yes |
| 1 | 00111 | Override Inhibit Terminal Flag Bit | No | Yes |
| 1 | 01000 | Reset Remote Terminal | No | Yes |
| 1 | 01001 | Reserved | No | TBD |
| 1 | 01111 | Reserved | No | TBD |
| 1 | 10000 | Transmit Vector Word | Yes | No |
| 0 | 10001 | Synchronize | Yes | Yes |
| 1 | 10010 | Transmit Last Command | Yes | No |
| 1 | 10011 | Transmit BIT Word | Yes | No |
| 0 | 10100 | Selected Transmitter Shutdown | Yes | Yes |
| 0 | 10101 | Override Selected Transmitter Shutdown | Yes | Yes |
| 1 or 0 | 10110 | Reserved | Yes | TBD |
| 1 or 0 | 1111 | Reserved | Yes | TBD |

NOTE: To be determined (TBD)

control functions over it. The various elements of the electrical control system communicate with each other via messages transferred on a standard DAIS 1553B multiplex data bus. Control and synchronization of the data bus is performed by the avionics processor. All electrical control system elements perform as remote terminals in relation to the avionics processor. Those elements that make up the electrical control system are the PSP, 5 ERTs, 3 DAIS RTs, 2 GCUs, avionics controls and displays, and a DAIS mass memory unit.

(1) Power System Processor

The PSP provides overall control of the electrical control system. Electrical system status information is provided to the PSP by other elements in the electrical control system. Avionics controls provide updated control and flight mode information whenever this information changes. The PSP uses this information it receives to calculate load management priority levels, power generation and distribution system configuration requirements, and electrical power request equation solutions. In addition to its control of the electrical control system during normal operations, the PSP also controls the electrical control system during system startup and shutdown operations.

(a) PSP Hardware Description

The PSP is an AN/AYK-15A digital processor with 128K 16 bit words of memory. This processor is described in DAIS specification SA 421205 (Reference 9). The primary function of the PSP is to provide control and management of the aircraft electrical system. To accomplish this, the PSP must perform several functions such as electrical generation network monitoring, electrical load priority establishment, power request equation solving, and power system startup and shutdown. In addition, the PSP must process requests from the DAIS 1553B bus controller and handle selected avionics data. A BIT capability is included in the PSP to insure integrity of the system.

(b) PSP Functional Requirements

Monitoring and control of the power distribution system requires the PSP to receive status inputs from both the electrical generation network and the

ERTs. The electrical generation network consists of all the aircraft generators, the aircraft external power source, the aircraft battery, and associated control units. Also included are both AC and DC power buses, and power controllers that provide routing of electrical power from the sources to the appropriate buses.

Status information received from the electrical generation network includes data from the GCUs, and the RT that monitors the APU and the aircraft external power source. Data received from the GCUs provides generator overload and failure status and PDS configuration status. Data received from the RT provides external power source status, and APU overload and failure status. Each ERT provides AC and DC feeder selection status for its ELMC. In addition, SSPC RESET and TRIP status is sent to the PSP. The flow of PSP control and status data is shown in Figure 21.

Under normal operating conditions each bus in the electrical generator network has a designated primary power source, and each ELMC has designated primary AC and DC feeders. Whenever generator failure occurs or sufficient overload conditions arise, automatic switching of power sources for one or more of the buses will occur and updated configuration and load status information will be sent to the PSP. Similarly, if an AC or DC feeder to an ELMC fails, automatic feeder selection will occur and updated status will be sent to the PSP. If electrical distribution network conditions cannot be successfully resolved automatically, then the PSP will override the automatic switching and modify the electrical distribution network as necessary.

Electrical Load Priority Establishment

Load priority establishment requires inputs from the electrical distribution network indicating generator configuration and condition. Inputs also must be received from the ERTs indicating AC and DC feeder selection. This information, combined with mission and flight phase data, and current state of the aircraft electrical system is provided to the PSP applications software to perform the calculations necessary to determine an appropriate electrical load priority level.

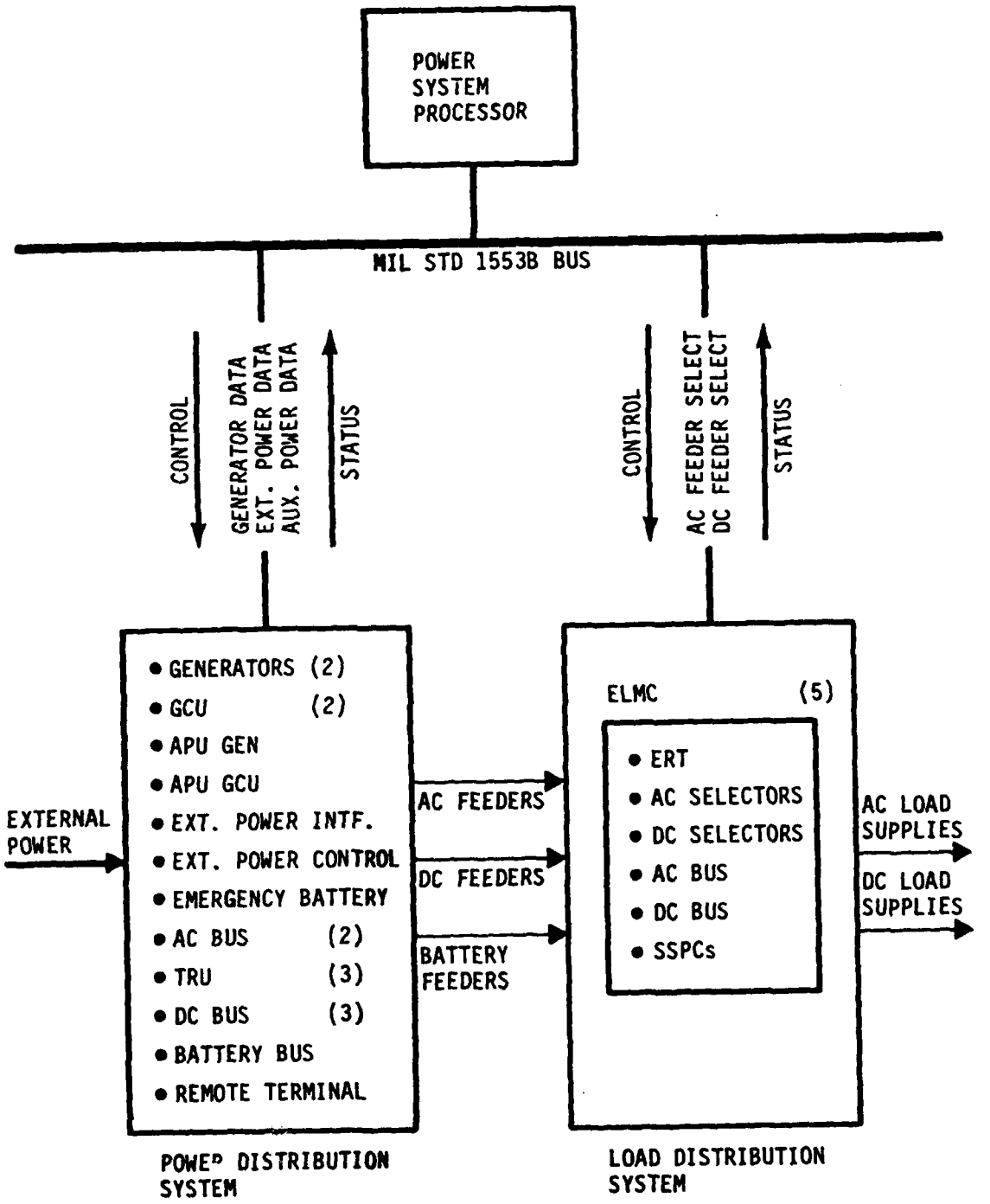



Figure 21 Power System Processor Control and Status Data Flow

Power Request Equation Solving

Power request equations are Boolean equations derived from aircraft discretes. Whenever power is needed for a particular aircraft function, the necessary power request equations are solved by the PSP applications software and appropriate power requests are issued to the ERTs for load priority analysis.

Power System Startup

The PSP controls power system initialization in order to insure that system power up occurs in an orderly fashion so as to prevent damage or failure of electrical equipment on the aircraft. Functions performed by the PSP at power system startup include BIT, initialization of ERTs, computation of initial load priority level, calculation of initial power request equations and transfer of the initial power requests to the ERTs.

Power System Shutdown

Similarly, power system shutdown must occur smoothly so as to prevent risk of damage or failure of aircraft electrical equipment. Power system shutdown requires the PSP to send final power requests and a shutdown message to the ERTs.

DAIS 1553B Bus Controller Request Processing

Bus controller request processing requires the PSP to respond to requests made by the avionics processor which controls the 1553B data bus. This function requires the PSP to perform various tasks such as providing controls and displays data, running BIT, enabling power to avionics subsystems, communicating with RTs or ERTs, and updating power system priorities. These tasks are performed by the PSP applications software.

(c) PSP Executive Software

The purpose of the PSP Executive (PSPE) is to provide an interface between hardware comprising the DAIS federated electrical power control system, and

the PSP applications software that executes in the DAIS processor. This interface permits applications software development without knowledge of the information transfer system hardware or its operation. Similarly, this allows hardware modifications to be performed without affecting the applications software since references to time or to RTs are on a logical level. The PSPE is basically the same as a standard DAIS single processor synchronous executive, (DAIS specification SA 221308, Reference 11), except that it does not perform data bus management, a function reserved for the avionics processor. The PSPE controls operations peculiar to the processor, including control of the PSP applications software and local participation in the I/O processes.

The architecture of the PSPE implies a separation of functional components, control of one component over another, and dependence of one component on another. The PSPE system architecture is shown in Figure 22 depicting the separation of hardware and software functions. The PSP applications software is functionally isolated from the hardware by the executive software just as the subsystems and EPTs are isolated from the computer by remote terminals and the data bus, respectively.

The PSPE is a realtime system, in which the activities of the PSP applications software are coordinated with the passage of real time in the outer world. The minimum quantum of time to which coordination occurs is known as the minor cycle. It is possible to specify or determine the time of an action within one minor cycle, but not to a fraciton of a minor cycle. Thus, I/O interactions and task interactions may occur, may be known, and may be controlled within the framework of the minor cycle time unit. This timing is a requirement for I/O control, synchronization and executive process handling.

In order to successfully control activities of the PSP applications software, the PSPE performs several functions. These functions include task control, event handling, compool block handling, executive control, minor cycle setup, and local initialization. These functions are discussed below.

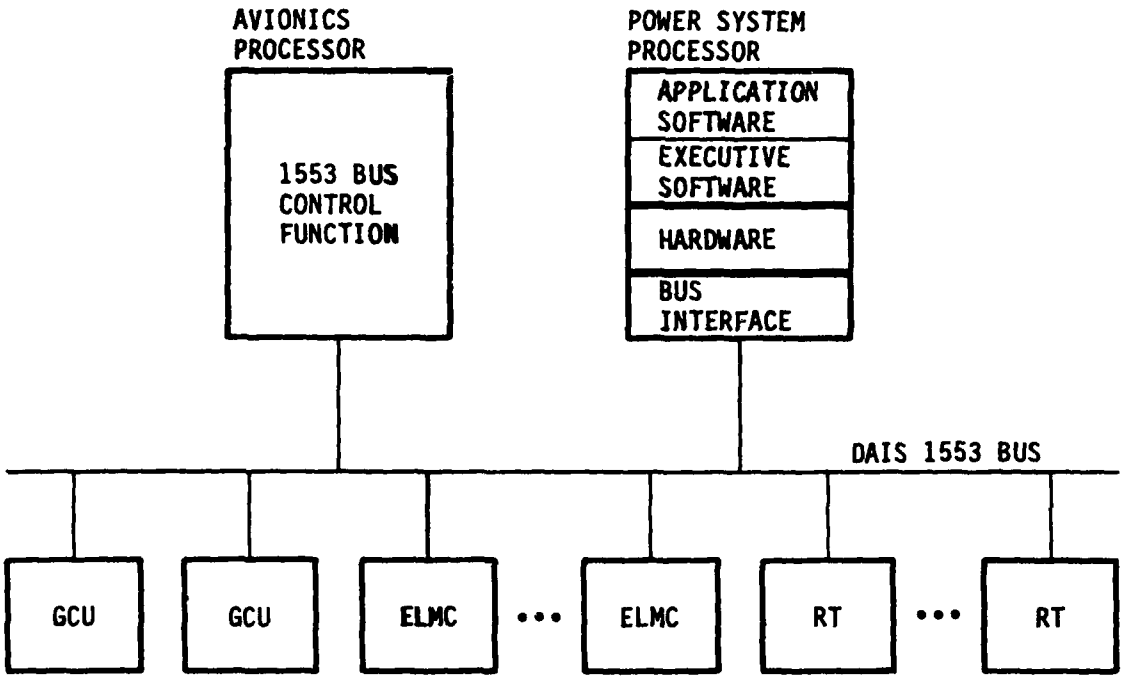



Figure 22 Power System Processor Architecture With PSPE

## Task Control

Tasks are processing modules that can be controlled and executed independently. In order to understand the interactions of tasks, it is necessary to understand possible "states" that these dynamic processes may have. At any given instant, each task in the PSPE mission software system has one of the "states" shown in Figure 23. It should be noted that not all states are mutually exclusive; in Figure 23, the tree structure shows a subsetting relationship with respect to the various states. Thus, INACTIVE and ACTIVE are both substates of INVOKED, and hence, a task which is INACTIVE (or ACTIVE) is simultaneously also in the INVOKED state. Similarly, a task that is SUSPENDED is also INVOKED, ACTIVE, and DISPATCHABLE.

Figure 24 also indicates the method of transition from one state to another. Figure 24 is another way of showing the state transitions. For example, a SCHEDULE statement will transfer an UNINVOKED task into an INVOKED state, while a CANCEL statement will transfer an INVOKED task into an UNINVOKED state.

o Task Hierarchy

Any given task may be SCHEDULED by one and only one task, which is called its controller. All tasks scheduled by a controller are said to be its "immediate descendants." Any immediate descendant can, in turn, be a controller for other tasks. The "descendants" of a task are its immediate descendants and all of the descendants which they have. The relationships of controller and descendant define task hierarchy.

o Priorities

At any time, there may be many processes potentially executable. These include tasks, executive actions invoked by tasks within the processor, and executive actions invoked by RTs and ELMCs. In order to resolve conflicting demands on the processor, a system of priorities has been adopted. Tasks are divided into two classes: normal mode tasks and privileged mode tasks. As a class, privileged mode tasks and executive actions have a higher priority than normal mode tasks. Within each class, conflicting demands on the CPU are resolved as described below.

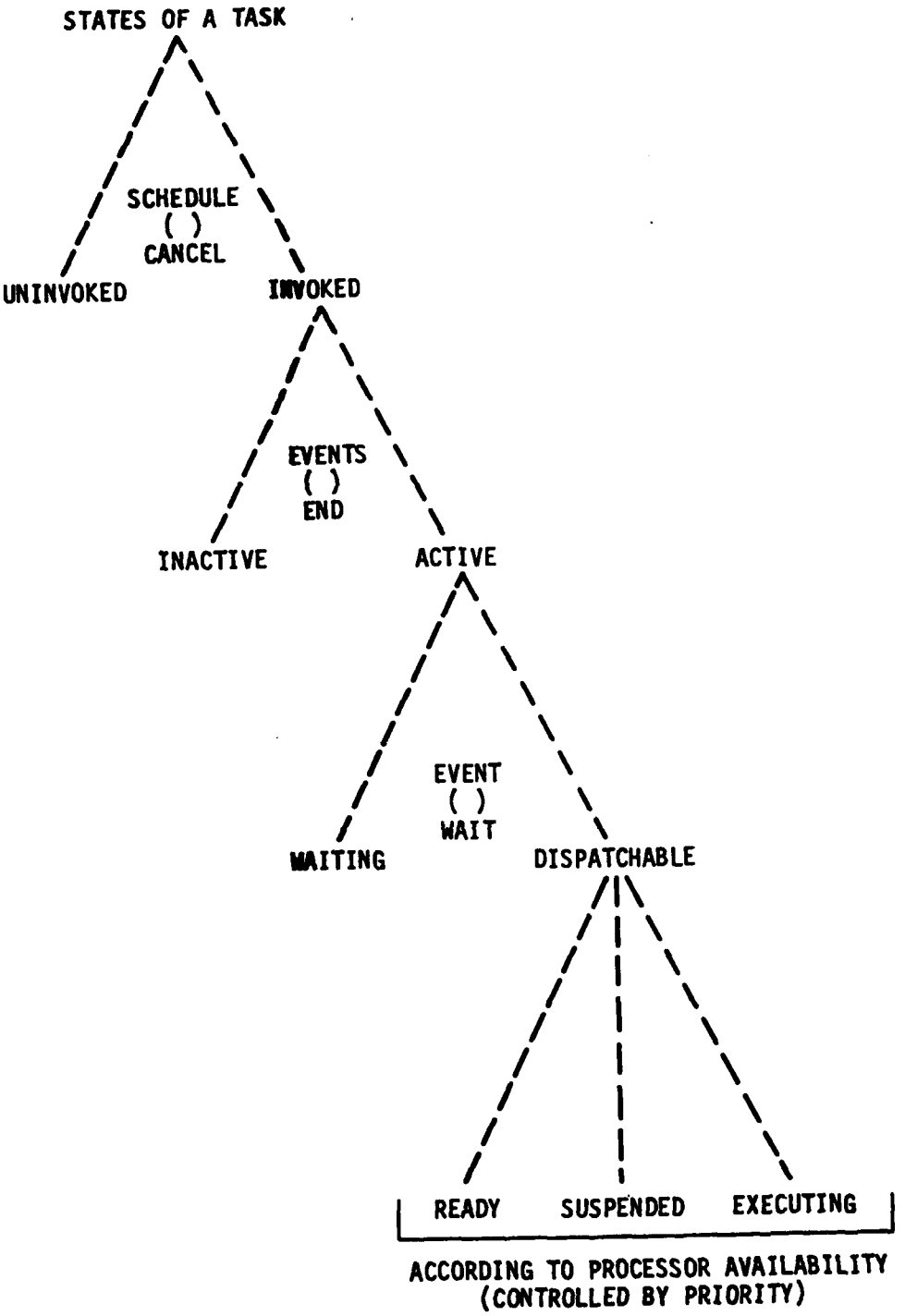



Figure 23 Task States

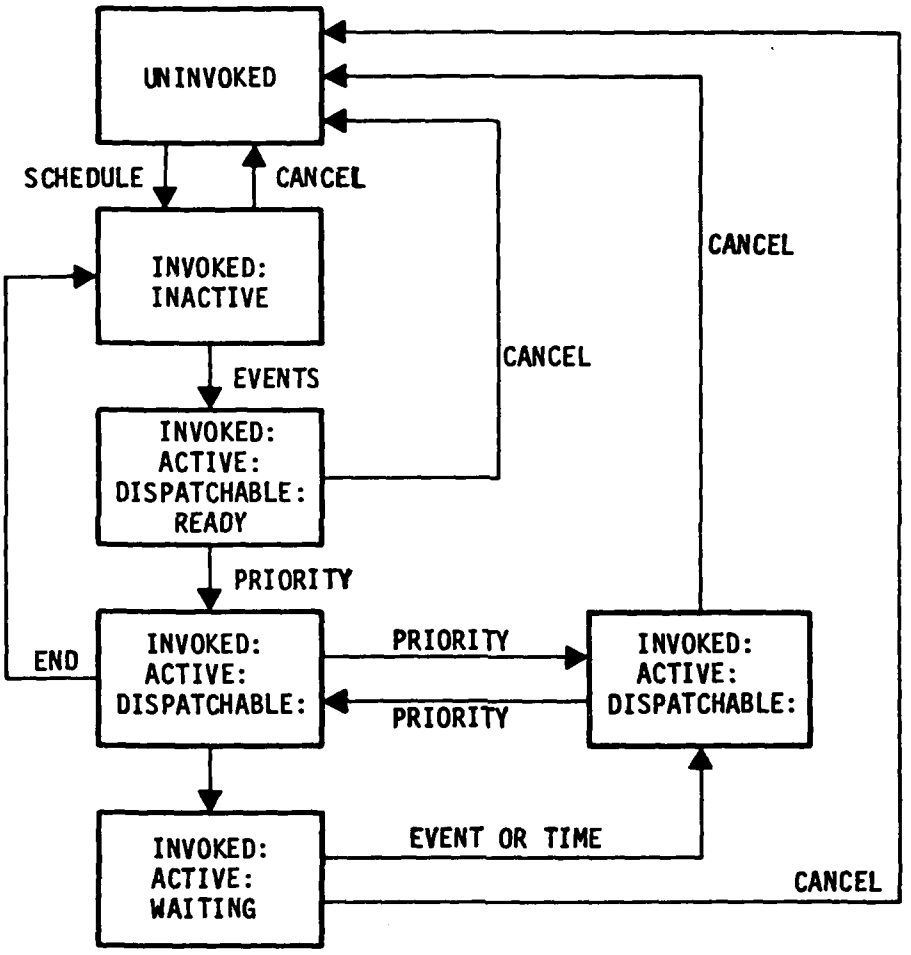



Figure 24 Task State Transition Diagram

Normal mode tasks are linearly ordered by priority. At any time, if no executive actions are called for and if no privileged mode tasks are ACTIVE, the CPU executes the highest priority ACTIVE normal mode task. If, during execution of a normal mode task, an executive action is called for or if a privileged mode task or a normal mode task with higher priority becomes active, the original task is immediately placed into SUSPENDED state.

Privileged mode tasks are not ordered by relative priority; instead, they are executed on a first come, first served basis. When a privileged mode task becomes ACTIVE, it is executed immediately. Once a privileged mode task is in EXECUTING state, it is in control of the processor. It can be SUSPENDED only when it invokes an executive action by means of a realtime statement. Upon completion of the action, control is returned to the task.

Event Handling

An event is a Boolean flag that may be referenced by one or more tasks. Events are used primarily to control the states of tasks, although they may also be used simply for communication of Boolean data. A task may SIGNAL an event, may read the values of an event, may WAIT for an event, and an event may appear in the event condition set of a task. Events are divided into two classes, explicit and implicit.

Explicit events are named and used by the applications software programmer. They contain the meaning which is assigned to them. The values of explicit events are determined solely by their initial state (OFF), and the values given to them by tasks. Implicit events are associated with certain system occurrences. Their values are not under the control of tasks, but are determined entirely by system occurrences with which they are associated. There are three categories of implicit events, namely task activitation events, COMPOOL block update events and minor cycle events.

Every task has an event condition set, which is used to control its activation. An event condition set is a collection of conditions, each one of which has, at any particular time, the value ON or OFF. Each condition also has a prespecified "desired" value, either ON or OFF. When all the conditions

of a task which is INVOKED but INACTIVE have their desired values, the task is activited (i.e., made ACTIVE). A task may have a null event condition set, in which case it can be INACTIVE only momentarily.

## COMPOOL Block Handling

COMPOOL blocks are data agglomerates used for communication between separate tasks and for communications between tasks and the external environment (i.e., RTs and ERTs). COMPOOL blocks are divided into three categories: input, output and intertask. Input COMPOOL blocks are used to input data from RTs and ERTs, which may then be used by tasks. Output COMPOOL blocks are set by tasks, and their values are output to RTs and ERTs. Intertask COMPOOL blocks are used for communications between tasks.

Since a COMPOOL block has a global copy in the processor, and also, possibly, a virtual copy in an RT or ERT, it is necessary to send COMPOOL update messages across the data bus to maintain consistency between the copies. COMPOOL blocks are classified as synchronous or asynchronous.

The various categories of COMPOOL blocks, and the ways in which they may be referenced by tasks, are shown in Table 7.

Table 7. CATEGORIES OF COMPOOL BLOCKS

| CATEGORY | SYNCHRONOUS | ASYNCHRONOUS |
|---|---|---|
| INPUT | May be used in many tasks. | Not used. |
| OUTPUT | May be set in one task. | Not used. |
| INTERTASK | May be set in one task.<br>Used in many tasks. | May be set in many tasks.<br>Used in many tasks. |

## Executive Control

The PSPE controls the state of realtime entities existing within the processor; specifically, tasks, global copies, and copies of events. The local executive control function is invoked at all points when a decision must be

made regarding what to process next, namely when an executive service has been completed. If no minor cycles are pending processing, then the local executive dispatches the highest priority DISPATCHABLE task. When a task has completed execution, it returns to the local executive control function. At this point, the task is set INACTIVE, and its activation event, if any, is signalled OFF. Then the task's event condition set is evaluated and the task is reactivated if all conditions are satisfied.

Local Initialization

Local initialization sets the time and minor cycle count to zero, and initializes internal variables indicating the executive state to null values. Processing of hardware errors is performed,and control is returned to the master sequencer routine.

(d) PSP Applications Software

The PSP applications software resides in the power system processor and executes under control of the PSPE. Functions performed by the PSP applications software include the following:

Power system startup
Power system shutdown
Electrical load priority establishment
Power request equation solving
Bus message processing
ERT status processing
Power distribution system configuration control
Controls and displays data handling

In order to perform its functions, the PSP applications software communicates with other elements in the DAIS federated architecture that comprises the aircraft electrical control system. The relationship and data flow between the PSP applications software and the other system elements is shown in Figure 25. As shown in Figure 25 the PSP applications software communicates with the avionics processor, generator control units, ERTs and electrical system RTs

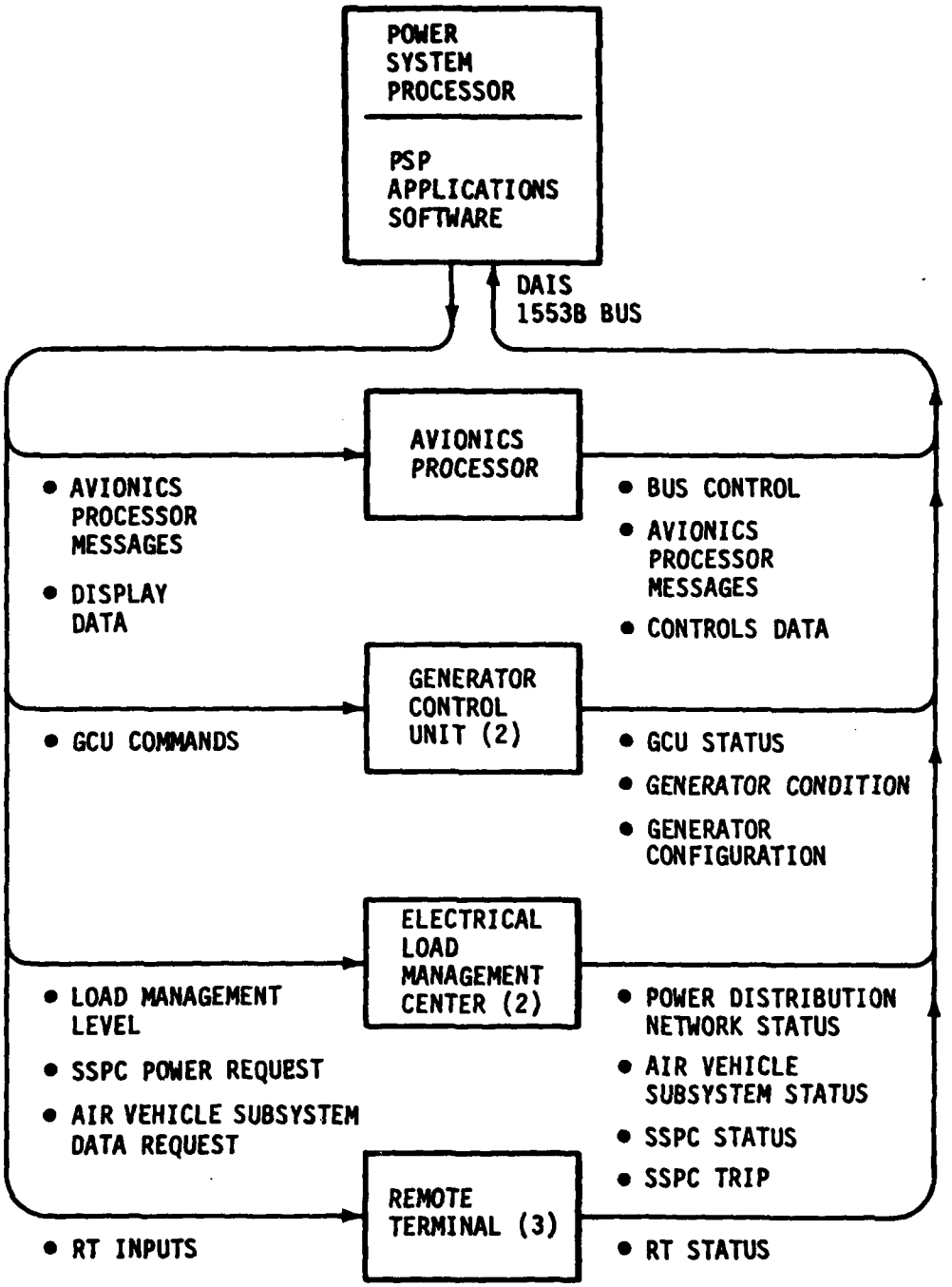



Figure 25 PSP Architectures Software Data Flow

via a DAIS 1553B data bus. The interface between the PSP applications software and the data bus consists of the PSPE, and the power system processor bus interface hardware. Functions performed by the PSP applications software are described below.

Power System Startup

The power system startup software module performs functions necessary to insure an orderly power up sequence of air vehicle equipments. First of all, the PSP applications software is initialized and an initialization message is sent to the ERTs. Next, initial power distribution system information, and aircraft mission and flight phase information are processed to determine an initial electrical load management priority level. This load management level is then sent via the 1553B data bus to the ERTs. Finally, initial power request equations are solved and requests for power are transferred to the ERTs.

Power System Shutdown

The power system shutdown software module sends equipment power off requests to the ERTs to insure an orderly shutdown of aircraft electrical power systems.

Electrical Load Priority Establishment

The load priority software module determines an appropriate electrical load priority level based upon generator configuration, generator condition, ELMC power bus connection, current state of the system and aircraft mission and flight phase. Whenever any of the above conditions changes, load management level equations are solved to provide a correct load management level which is then sent to the ERTs. There are 16 possible load management levels. Load management level selection is depicted in Figure 6.

Power Request Equation Solving

Power request equations are of the form Z=R where R may take one of the following forms:

| | |
|---|---|
| Form 1 | One variable of the form A or $\bar{A}$, or the value "logic 1" |
| Form 2 | Five variables arranged in any valid Boolean expression with each variable used once, only |
| Form 3 | Twenty variables arranged in any valid Boolean expression with each variable used once, only |
| Form 4 | Two hundred variables arranged as the sum of products with each product term composed of no more than six variables with no variable repeated in the Boolean expression |

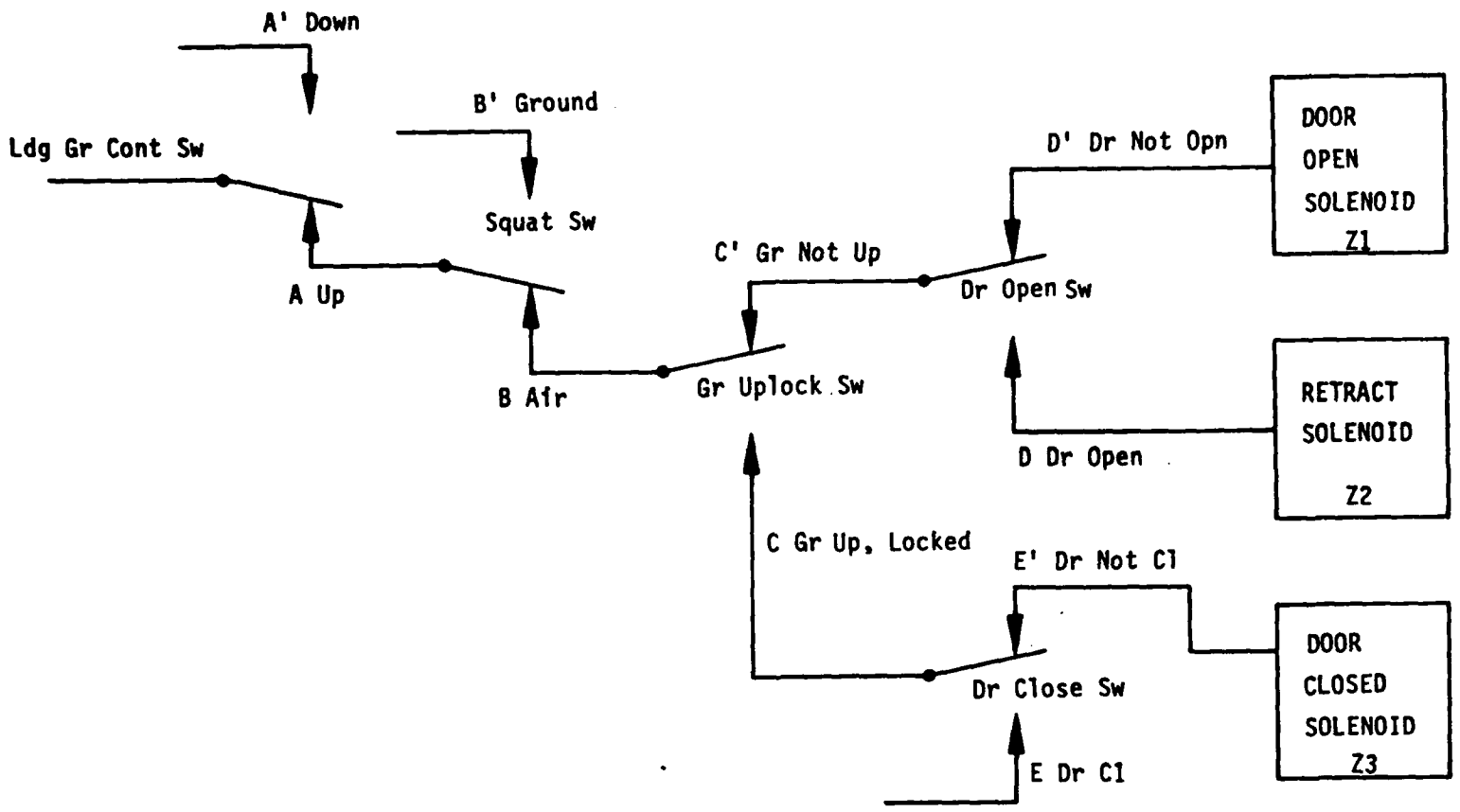
There will be approximately 208 form 1, 236 form 2, 45 form 3, and 8 form 4 equations for this aircraft. Figure 26 shows an example of how typical power request equations are derived from various airplane discretes. Power request equations are solved by performing required Boolean operations on the equation parameters. After the equations are solved, results are sent via the 1553B data bus to the appropriate ERT where the results are used for computing load control equations.

Bus Message Processing

The bus message processing software module receives messages from the DAIS 1553B data bus, determines the message function and calls the appropriate software module to process the message. Bus message types and appropriate bus message processing actions are described below.

- Request avionics data
  Call avionics data handling module to collect appropriate avionics data from power system RTs.

- Request displays data
  Call controls and displays module to send displays data to avionics processor.




A = Landing Gear Handle UP
B = Air Vehicle Airborne
C' = Landing Gear Not UP
D' = Door Not Open
E' = Door Not Closed

Z1 = A•B•C'•D' Energizes door open solenoid
Z2 = A•B•C'•D Energizes gear retract solenoid
Z3 = A•B•C •E' Energizes door close solenoid

where Z = the summation, result or response
and • = "and" (rather than "or")

Figure 26 Power Request Equation Example

- o Controls data
  Call controls and displays module to process controls data.

- o Commands received
  Power system startup -- call power system startup
  Power system shutdown -- call power system shutdown
  Run BIT -- call BIT module.

- o Data received
  Aircraft mission
  Aircraft flight phase
  Power generation system condition -- call load management priority level module

- o Request for power
  Call power request equation solving module

- o ELMC status
  Call ELMC status update module

ERT Status Processing

The ERT status processing software module updates electrical power system parameter tables using SSPC TRIP and RESET status provided by the ERTs.

Power Distribution System Configuration Control

The power distribution system configuration control software module determines the most appropriate configuration for the power distribution system based on current system status, and current aircraft mission and flight phase. As shown in Figure 27, inputs to this software include power distribution system configuration, capacity and loading status, and aircraft mission and flight phase. The software determines the maximum available power by generator, and for the total generation system. This capacity is compared to the needs for the current aircraft mission, flight phase, and electrical load priority level. If insufficient total generation capacity exists, the electrical load

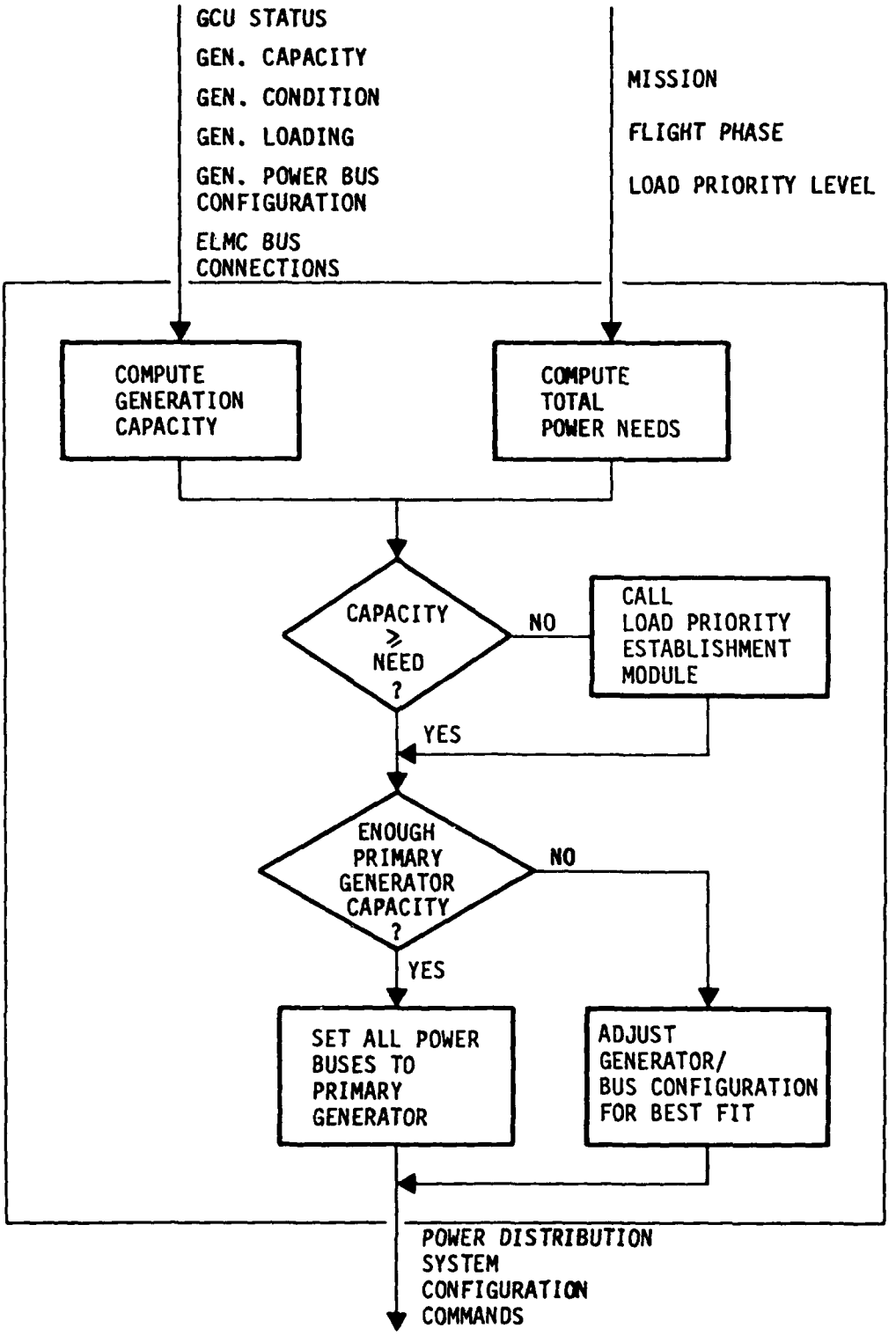



Figure 27 Power Distribution System Configuration Control

priority establishment software module is called to assign a new load management level. Next, the software determines if the currently designated primary generator has sufficient capacity to meet existing load levels. If it does, the power distribution system is configured so that all loads run off the primary generator. If not, the power distribution system is reconfigured for an optimum load mix using the available generators.

Controls and Displays

The aircraft controls and displays interface to the electrical control system through the avionics processor. Electrical control system information that is to be placed on the aircraft displays is sent to the avionics processor. Similarly, control information received from the aircraft controls is received by the avionics processor and that information which affects the aircraft electrical control system is sent to the PSP via the multiplex data bus.

(2) Electrical Load Management Center

The ELMCs provide control and management of the electrical power distributed to the loads connected to them. The ELMCs contain SSPCs from which it receives status information and sends control information. The ELMCs interface with the power system processor, via the MIL-STD-1553B data bus. Each ELMC contains an imbedded electrical remote terminal (ERT). Control of the ELMC, its I/O, subsystems, and bus interface is handled by a microprocessor within the ERT. The ELMC design will be modular and flexible to allow signal handling to be incrementally expanded or contracted in order to accommodate the requirements of a particular load configuration. Figure 28 is an ELMC functional diagram.

Tasks 1 and 2 resulted in an initial ELMC configuration containing 100 SSPCs; however, further studies during preliminary design indicated potential interface wiring problems with packaging 100 SSPCs in a single box. This problem may be alleviated by changing the SSPC control interface from a four-wire method to a two-wire method. The four-wire method is a discrete signal interface and the two-wire method is an analog interface. In both methods, a control ON/OFF signal is sent to the SSPC and a TRIP and STATUS signal is

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ADVANCED AIRCRAFT ELECTRICAL SYSTEM CONTROL TECHNOLOGY DEMONSTR--ETC(U)
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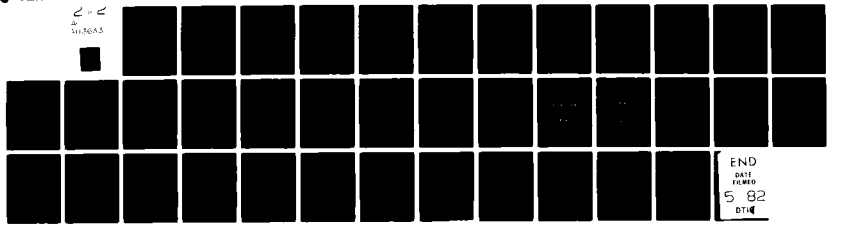

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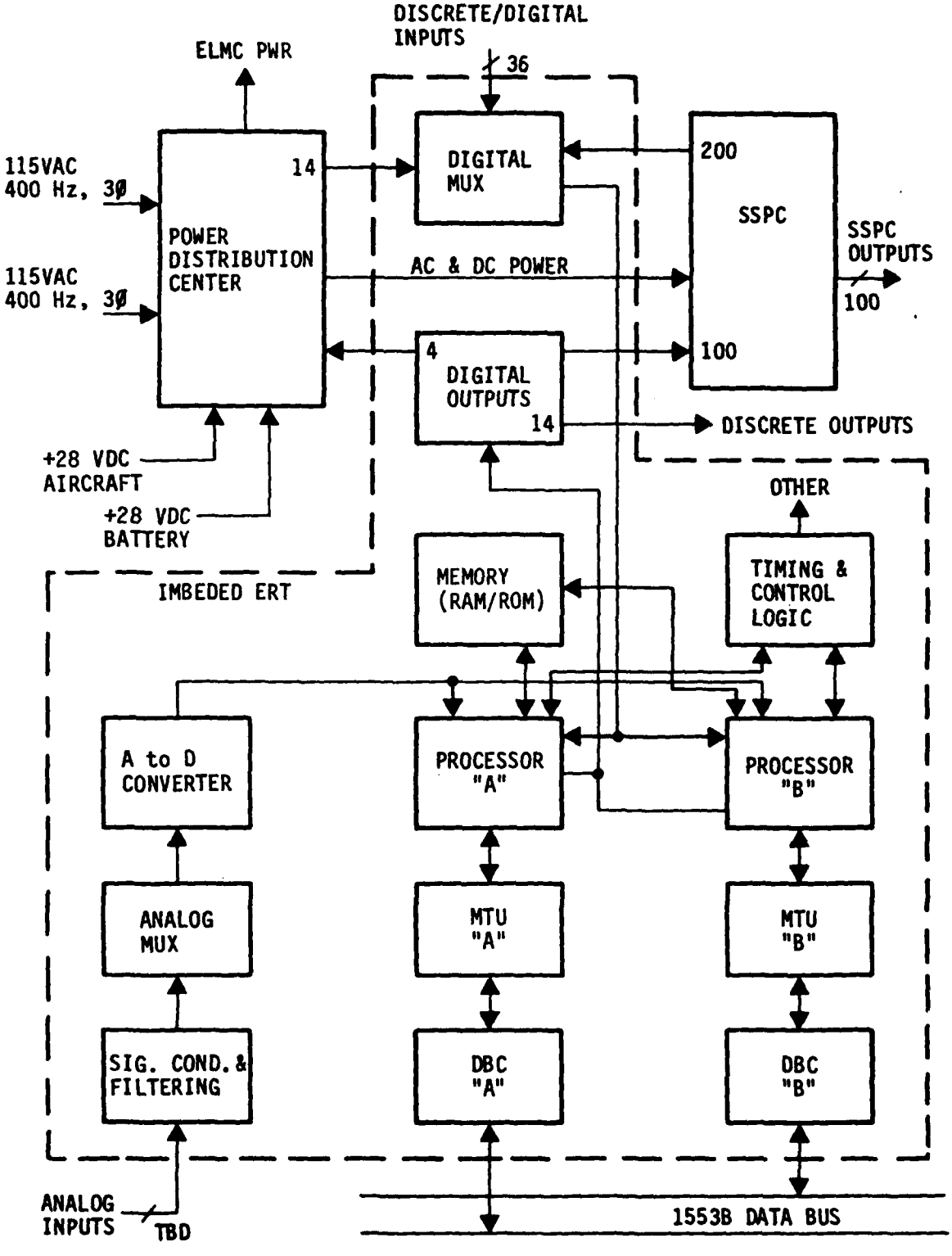



Figure 28 ELMC Functional Diagram

received. If this problem results in a reduction in the number of SSPCs packaged in an ELMC, the number of ELMCs in the system will increase. This in turn results in a slight increase in avionics processor overhead and bus loading caused by the increased number of addressable devices attached to the bus. The impact on the electrical control system bus traffic is minimal since the total number of SSPCs to be controlled and monitored is unchanged.

The main purpose of the ELMCs is to provide electrical power as needed to aircraft subsystems, consistent with the current electrical load management priority level. This purpose is achieved by accomplishing several functions including power bus control and monitoring, SSPC control and monitoring, aircraft discrete and analog signal monitoring, ERT software computations, and BIT.

(a) ELMC Functional Description

The power distribution center as depicted in Figure 29 provides automatic selection of power sources for the ELMC AC and DC buses. All power buses within the ELMC have two sources of power, of which one source is designated the primary source and the other is designated the secondary source. Under normal operating conditions, power to each bus is supplied by the primary source. If the primary source fails, power is automatically provided by the secondary source. Precautions will be taken to insure that two sources are not connected to a particular bus at the same time. Selection of power sources can also be done by control of the ERT computer. In the case of the flight critical bus, the primary power source is the DC bus which is powered by either its own primary or secondary source, and the secondary power source is an emergency battery. This battery is diode-paralleled with the primary source to insure that the battery is isolated from faults in the main DC system.

(b) SSPC Control and Monitoring

The SSPC control unit receives control inputs from the ERT, outputs SSPC status to the ERT, and controls the power supplied to various aircraft loads with SSPCs. The SSPC control unit is capable of solving Boolean equations

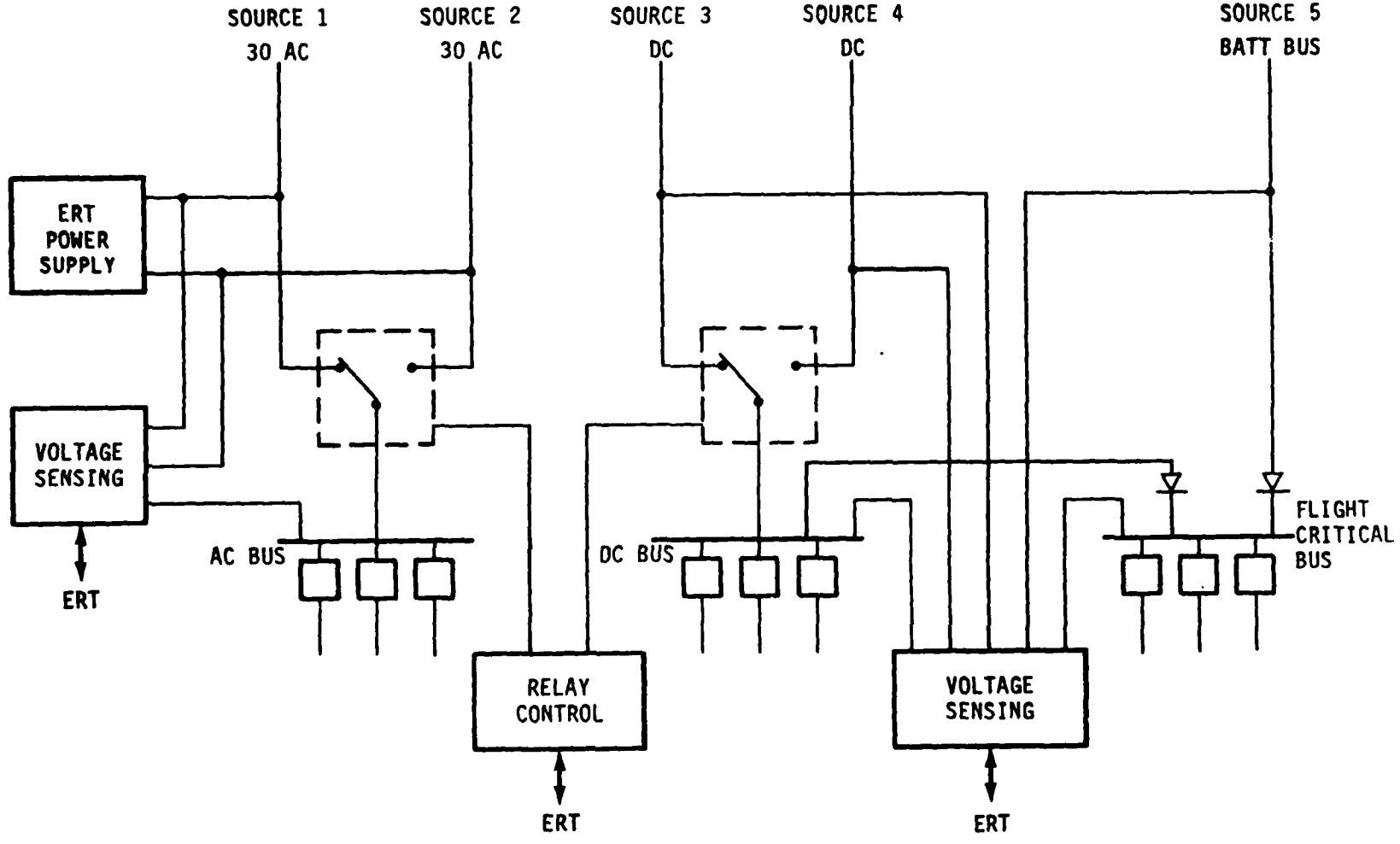



Figure 29 ELMC Power Distribution Center

used to control the SSPCs. Each SSPC is controlled by a single ON/OFF signal and provides a TRIP signal and an ON/OFF status signal.

(c) Aircraft Discrete and Analog Signal Monitoring

The ERT samples, converts, and formats AC and DC analog and discrete signals from the SSPC and aircraft subsystem interfaces. The formatted values are then sent as messages on the 1553B data bus upon receipt of a command to do so. Similarly, the ERT receives messages from the 1553B data bus and reflects the messages as discrete output signals to the SSPCs and subsystems. When required, the ERT retains signal levels until they are changed by another message.

(d) ERT Software Computations

ERT software computations include load priority handling, power control equation solving, power system status equation solving, and 1553B bus communications. These functions are discussed under ERT software functions.

(e) Built In Test

BIT as performed by the ERT will include tests of SSPCs and interface modules.

(3) Power Controllers

(a) Solid State Power Controllers

Solid state power controllers (SSPC) are used to control power to aircraft loads. The SSPCs also provide overcurrent and fault protection for the individual load feeders. The SSPCs are mounted on circuit cards in the ELMCs. The ERT provides the data bus interface for the SSPCs.

SSPC Distribution

500 SSPCs are used in the AAES, 100 in each ELMC. This includes AC and DC SSPCs. All AC SSPCs are single phase. Three phase loads will be controlled

by three single-phase SSPCs which, through control software, will be treated as one three phase SSPC.

SSPC Characteristics

The AC and DC SSPCs will be mounted on cards in the ELMC. The card will be a line replaceable unit. Heat from the SSPCs will be dissipated through the mounting side rails for the cards.

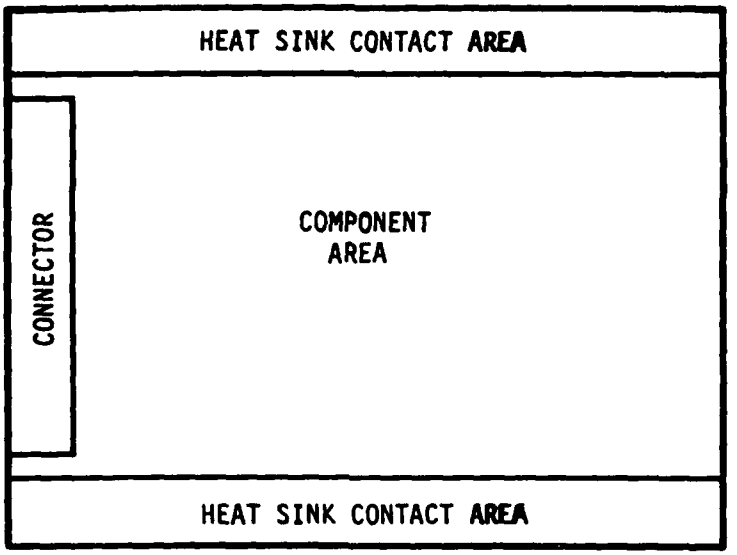
A four wire interface is used for each SSPC. This interface consists of a control line, status line, trip line and signal ground line. These control lines provide for the ON, OFF command signals and the status signals, ON, OFF, and TRIP. Figure 30 shows the SSPC configuration and the SSPC circuit card.

SSPCs can be made indifferent to system rupture capacity through current limiting or instantaneous trip. Instant trip has been selected for this system since it is more cost effective than full current limiting. No coordination is required since the SSPCs are restricted to the lowest tier of power switching.

The level of instant trip is subject to trade offs. A 15 X level is required for universal application. For the incandescent type loads which require that level there is little problem; however, this is not the case for inductive type loads. If a primarily inductive overload is allowed to charge up to that level, which is more than 2 X the normal inductive surge, the energy that must be absorbed by the switching device is then greater than 4 X the normal maximum. Thus the preferred trade off is to set the instantaneous trip at 7.5 X. The incandescent type load then requires a 2 X rated circuit.

(b) Electro-Mechanical Power Controllers

EMPCs are used for control and protection of AC and DC power feeders to the ELMCs and TRUs. EMPCs are also used for load feeders on those loads requiring power controllers larger than 7.5 A AC or 20 A DC, such as fuel pumps. For high current multiple applications, the EMPC offers clear advantages. The power dissipation, voltage drop, and cost are relatively unaffected by the



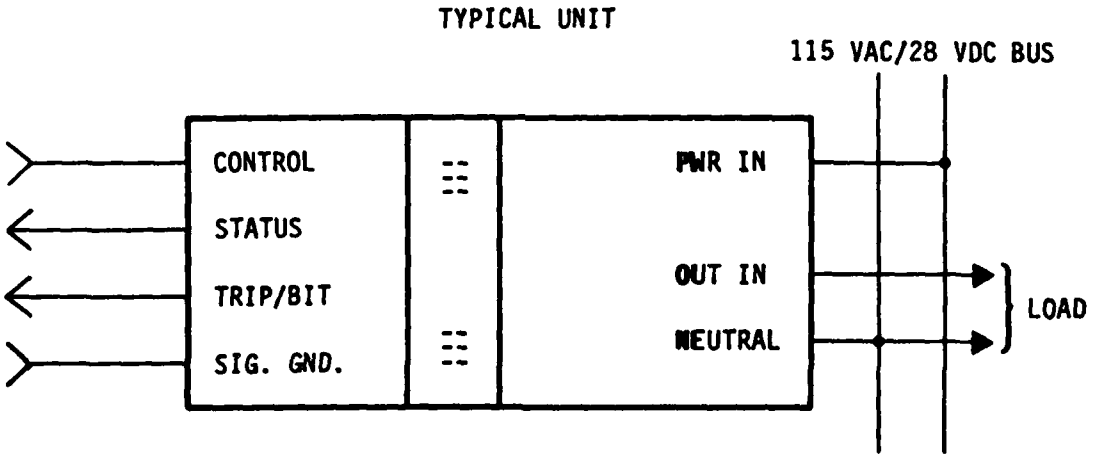




Figure 30 SSPC Circuit Card and Configuration

nominal current rating, over the range of 5 to 125 amperes. EMPC costs are primarily determined by rupture requirements.

The EMPCs will be interfaced to the data bus system through RTs. EMPCs used as feeder controllers will employ a "FAIL ON" type interface. This is a grounding signal for a close or ON command. The interface for the EMPCs has not been determined and requires further study.

(4) Electrical Pemote Terminal

The ERT provides the primary interface between air vehicle subsystem equipments, SSPCs and a MIL-STD-1553B data bus. In addition, the ERT provides the interface between various DAIS core elements. Major components of an ERT include discrete data I/O units, analog data input units, an imbedded microprocessor, a multiplex terminal unit (MTU), an I/O decode control unit and a power supply. Major ERT components and their functional relationship are shown in Figure 31.

Control of the ERT, its I/O subsystems, and bus interface is handled by an embedded microprocessor. This processor provides the necessary intelligence to the ERT for processing and controlling discrete inputs, discrete outputs and analog inputs. An ERT receives messages from the 1553B data bus and converts the information received to a form suitable for outputs as AC or DC analog, and discrete, synchro or serial digital signals to aircraft subsystems. Similarly, signals received from aircraft subsystems can be transformed by the ERT to a format suitable for inclusion in a message on the 1553B data bus. When required, an ERT can retain signal levels until they are changed by another bus message. Design of the ERT will be modular and flexible to allow signal handling to be incrementally expanded or contracted in order to satisfy the requirements of a particular geographical location.

(a) ERT Functional Description

ERT Processor

The ERT processor is a programmable general purpose microcomputer that

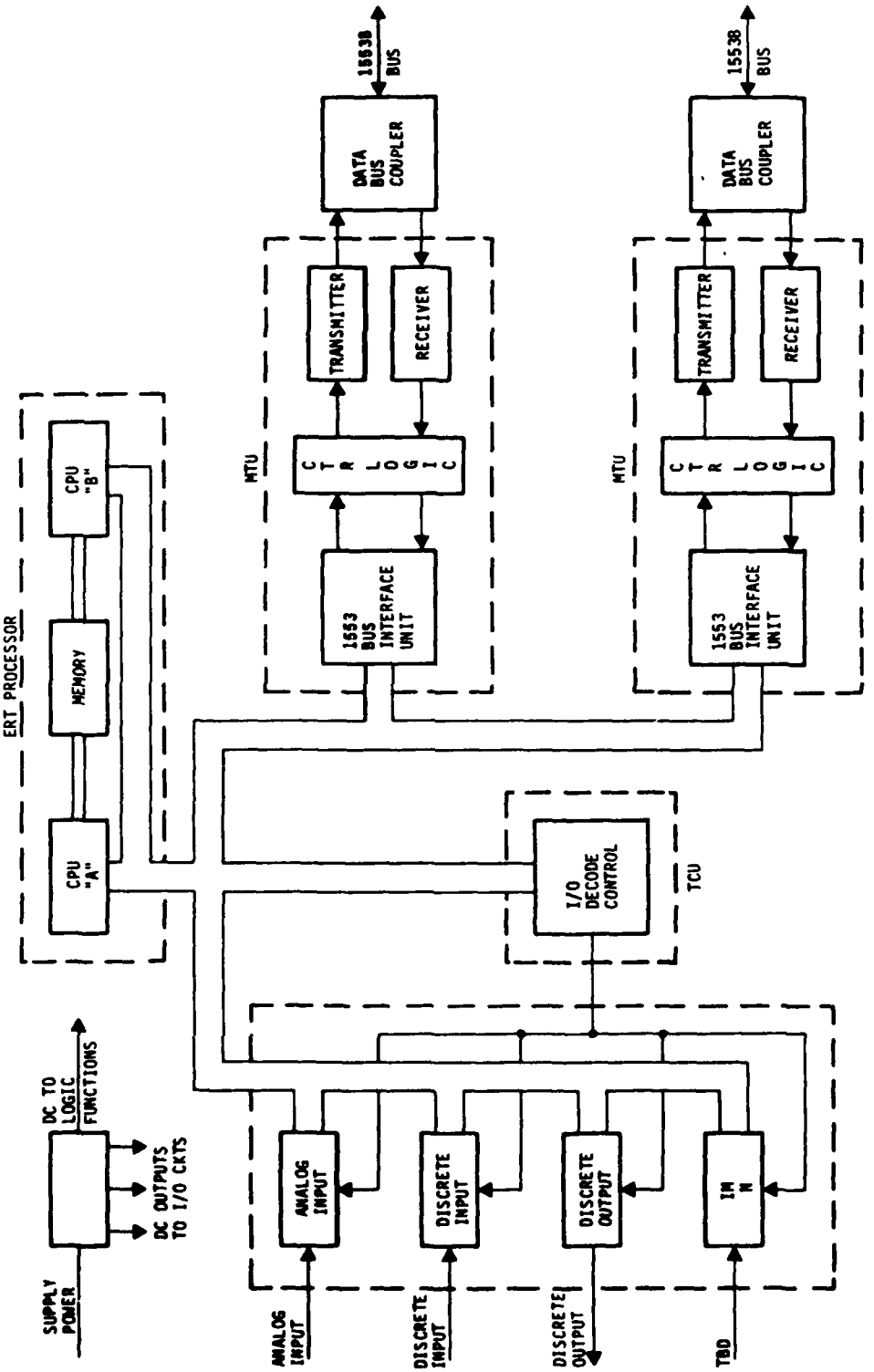



Figure 31 ERT Major Components

provides the data interface and control function between the MTU and air vehicle subsystems, and provides control of communications on the ERT local bus. Characteristics of the processor include the following:

16 bit word size
Arithmetic Operations (basic)
16 general purpose registers
Direct addressing to 64K bytes
Interrupt capability
Single supply voltage

The processor memory will contain both PROM and RAM of sufficient size to support the functions and operations of the ERT. The PROM card will be configured such that it can be addressed either as 64K 8 bit bytes or as 32K 16 bit words. The RAM card will be configured so that it can be addressed as 16K 8 bit bytes or as 8K 16 bit bytes. Both memory types will have an access time sufficient to support the processor without creating "wait" states. A block diagram of the processor is shown in Figure 32. The single bidirectional 16-bit data bus serves as an interface between the CPU and the MTU data buffers and subsystem. The ERT processor is programmed to "personalize" each ERT according to the interface module mix as determined by subsystem requirements.

Currently, there does not exist a 16 bit microprocessor capable of executing the MIL-STD-1750 instruction set. It is anticipated that such a processor will become available in the next 2 to 3 years. Meanwhile, functions of the ERT can be implemented by using a Z8000 series microprocessor. A Jovial compiler is expected to be available for the Z8000 in 1982. Machine dependent code will have to be implemented in Z8000 assembly language.

Multiplex Terminal Unit

The Multiplex Terminal Unit (MTU) is designed to provide an interface between the ERT and the 1553B data bus and to support the bus protocol as defined in MIL-STD-1553B. The MTU contains a transmitter/receiver section, data bus coupler, and control logic. The MTU must first be programmed by the power system processor via the 1553B data bus to perform the following:

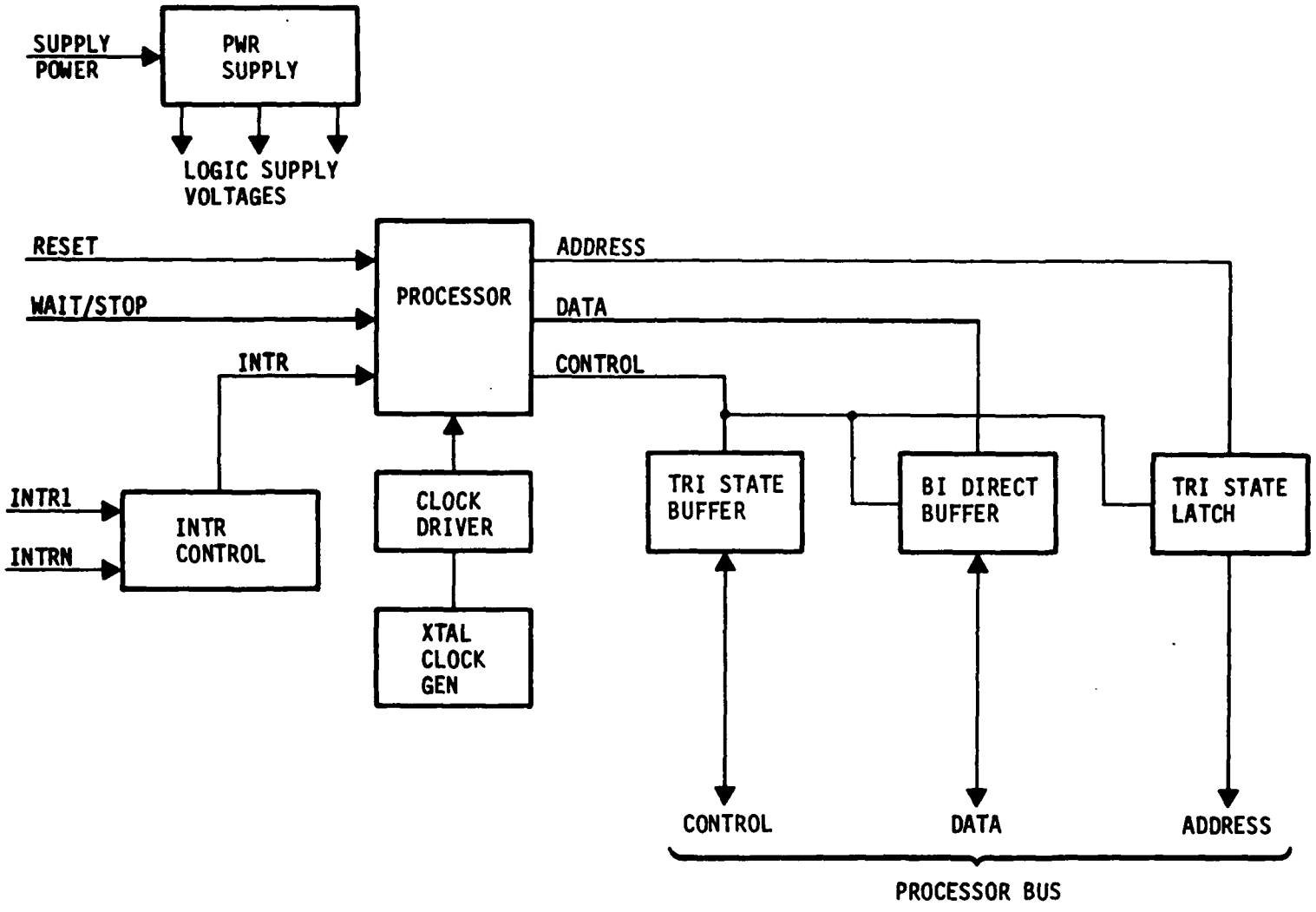



Figure 32 ERT Processor Functional Block Diagram

a) Output data
   1) Location
   2) Amount
b) Input data
   1) Location
   2) Amount

Once a remote MTU has been programmed, it monitors all bus traffic waiting for its specific address. After its address has been decoded, an MTU responds to the particular command being sent. An MTU also checks incoming data for parity, bit count, word count and protocol errors. The proper message sync, parity bits and status information are inserted into the response word by the MTU. Once a remote MTU has been initialized, it can execute an entire bus frame without processor intervention when commanded.

The transmitter/receiver portion of the MTU converts digital data to Manchester data for transmission on the bus. Manchester data is converted to digital data when received from the bus. The data bus coupler is a transformer coupled device that isolates the ERT from the main bus and provides proper matching impedances between the ERT and the data bus.

I/O Decode and Control

The ERT I/O decode and control section performs repetitive functions that need to be removed from processor operation. This circuitry is closely coupled with processor activity and is used by the main controlling function for routing data to and from digital I/O circuits.

Discrete I/O

The discrete input circuits will be capable of handling 250 inputs. These circuits provide necessary signal conditioning and supply conditioned digitized data to the processor under control of the I/O decode and control section. The discrete output circuits will be capable of handling 118 outputs. These circuits provide drive and signal characteristics required by the driven devices and receive data from the processor under control of the I/O decode and control section.

Analog Inputs

The analog input circuits will be capable of receiving 32 low level differential inputs or 64 high level single ended inputs. These circuits contain the electronics required to perform signal conditioning, mode selection, multiplexing and A/D conversion. Data received and converted is routed to the processor under control of the I/O decode and control section.

Power Supply

The power supply receives power from the aircraft power bus and converts it to regulated voltages required by the ERT. The power supply contains circuitry to inform the processor of a power shutdown or fault in order to allow graceful shutdown. A power on reset will be generated by the power supply.

(b) ERT Executive Software

The purpose of the ERT executive (ERTE) is to provide an interface between hardware comprising the electrical load management center, and the ERT applications software that executes in the ERT processor. This interface permits applications software development without knowledge of the information transfer system hardware or its operation. Similarly, this allows hardware modifications to be performed without affecting the applications software since references to time or to hardware devices are on a logical level. The ERTE is basically the same as a standard DAIS single processor synchronous executive (DAIS specification SA 221308), except that it does not perform data bus management, a function reserved for the avionics processor. The ERTE controls operations peculiar to the processor, including control of the ERT applications software and local participation in the I/C processes.

The architecture of the ERTE implies a separation of functional components, control of one component over another, and dependence of one component on another. The ELMC system architecture including the ERTE is shown in Figure 33 depicting the separation of hardware and software functions. As shown in Figure 33, ERT applications software is functionally isolated from the hardware by the executive software.

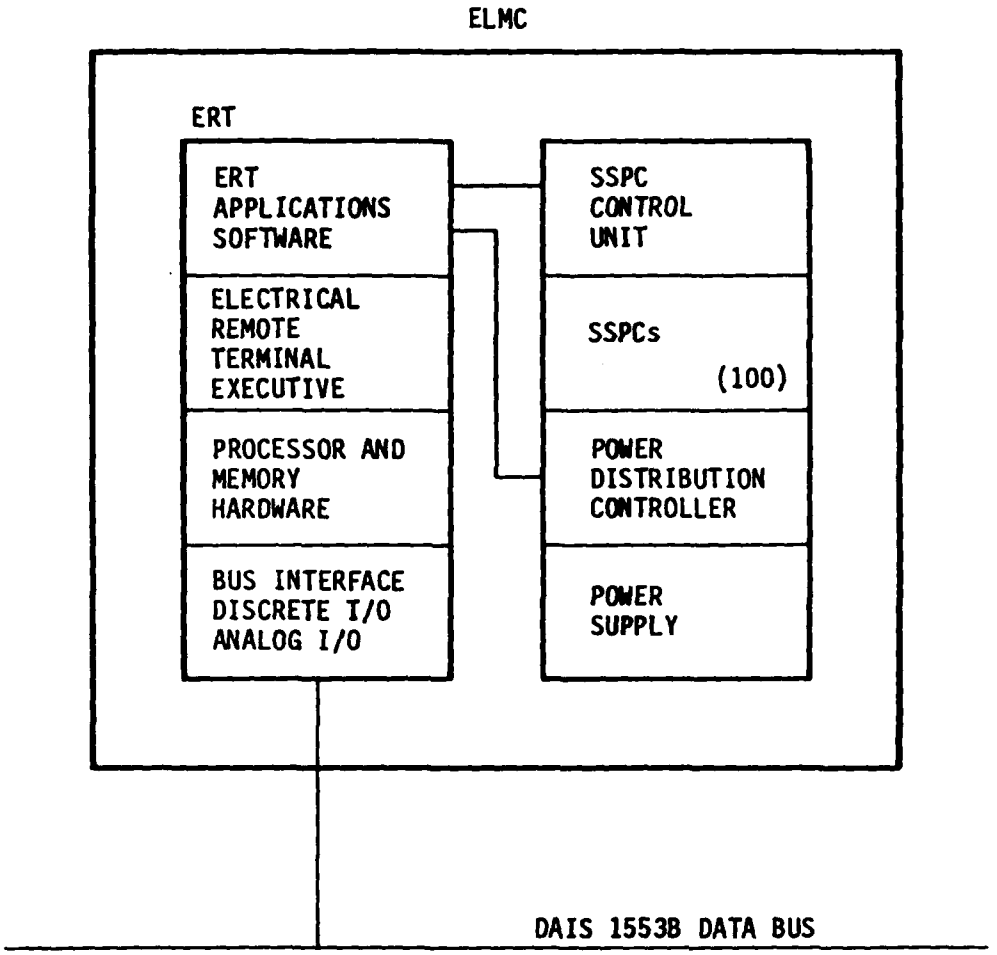



Figure 33 ELMC Architecture Including ERT Executive

The ERTE is a realtime system, in which the activities of the ERT applications software are coordinated with the passage of real time in the outer world. The minimum unit of time to which coordination occurs is known as the minor cycle. It is possible to specify or determine the time of an action within one minor cycle, but not to a fraction of a minor cycle. Thus, I/O interactions and task interactions may occur, may be known, and may be controlled within the framework of the minor cycle time unit. This timing is a requirement for I/O control, synchronization and executive process handling.

In order to successfully control activities of the ERT applications software, the ERTE performs several functions. These functions include task control, event handling, compool block handling, executive control, minor cycle setup, and local initialization. These functions are identical to the corresponding functions of the PSP executive, and are discussed in Section III.2.c.(1).(c), PSP Executive Software.

(c) ERT Applications Software

The main purpose of the ERT applications software is to control and monitor electrical power that is distributed to individual aircraft loads via SSPCs. This must be done in a manner consistent with the current load management priority level as determined by the PSP. The ERT applications software resides in the ERTs and executes under control of the ERTE. This software is table driven, and those tables that are unique to individual ERTs are loaded from the DAIS mass memory unit at system initialization time. This provision allows identical program code to be used in all ERTs. To accomplish its purpose, the ERT applications software must perform several different functions. Functions to be performed include the following:

ERT startup
ERT shutdown
Power bus control and status monitoring
Load priorities handling
SSPC control equation solving
SSPC status equation solving

Aircraft sensor discretes monitoring
1553B data bus message handling

These functions are described below.

ERT Startup

ERT startup occurs when the ERT executive receives an initialization request from the PSP applications software. When this happens, the aircraft electrical control system is initialized as follows. Load management tables are down loaded from the PSP via the DAIS 1553B data bus. An ERT ready status is sent to the PSP.

ERT Shutdown

ERT shutdown occurs when the ERT executive receives a shutdown request from the PSP applications software. When this occurs, all outstanding power requests are completed, and a completion message is sent to the PSP. No additional power requests or load management level changes will be accepted until the ERT receives an initialization request.

Power Bus Control and Status Monitoring

The power distribution controller, shown in Figure 29 provides automatic selection of power sources for the ELMC AC and DC buses. Whenever automatic power source selection occurs, a status flag bit is altered so that this software module can detect current status. This status is then sent to the PSP via a DAIS 1553B bus message.

The PSP applications software uses ELMC feeder selection status when analyzing power distribution network configuration. If a power distribution network reconfiguration occurs, and if this results in required changes to ELMC feeder selection, a DAIS 1553B data bus message is sent to the appropriate ERTs. This message is interpreted by the power bus control and monitoring software which then overrides the automatic power feeder selection and causes a change in ELMC power sources to occur. A message giving updated feeder selection status is returned to the PSP applications software.

Load Priorities Handling

Load priorities handling occurs whenever a message is received from the PSP applications software, indicating that a new electrical load management priority level is in effect. This software module saves the new priority level and then calls the SSPC control software module to RESET any SSPCs that are currently set, but are not allowed to be SET under the new load priority level.

SSPC Control Equation Solving

SSPC control equations must be solved whenever a request for power message is received from the PSP, or whenever a new load management priority level is implemented. For each ERT there are a maximum of 100 SSPC control equations of the form:

$$C = \overline{L}P\ (R + Q)$$

Where P is a single variable, L is the solution to the latch equation, Q is a test request, and R is a request bit obtained from the PSP applications software.

SSPC Status Equation Solving

Power system status equations are solved whenever status changes occur with the SSPCs, or when requested by the PSP applications software. Each ERT has 100 power system status equations of the form:

$$I = (L + PX)$$

where L is defined as in power system control equations above; P, and X are single variables available to the system designer for definition.

Aircraft Sensor Discretes Monitoring

Aircraft sensor discretes are collected and sent to the PSP.

1553B Data Bus Message Handling

The 1553B data bus message handling software module periodically checks the message input buffer and reads any messages that have been placed there. Each message is decoded to determine its function, and the appropriate software module is called to process it. The data bus message handling module is also called by other software modules to format output messages for transmissions on the 1553B data bus. Bus messages received and the corresponding actions taken are listed below.

ERT startup
    call ERT startup module
ERT shutdown
    call ERT shutdown module
Power bus feeder select
    call power bus control and status monitoring module
Power request matrix
    call SSPC control equation solving module
Load management priority level
    call load priorities handling module

(5) Remote Terminal

Standard DAIS RTs will be used where the intelligence provided by ERTs is not needed. As such, RTs will be used to provide interfaces between air vehicle subsystem equipments and the MIL-STD-1553B data bus. Also, RTs will provide an interface between the power distribution system and the 1553B data bus. The RTs will conform to the DAIS standard design as defined in DAIS specification SA 321 301 (Reference 12). Major RT components include multiplex terminal units (MTU), timing and control unit (TCU), and interface modules (IM).

Multiplex Terminal Unit

The MTU forms the communication path between the TCU and the 1553B data bus. The MTU receives control and information signals from the TCU and, based upon

these signals, performs transmit operations on the 1553B data bus. Conversely, the MTU accepts data bus words and generates control and information signals to the TCU for the purpose of passing received data bus words to the TCU.

Timing and Control Unit

The TCU consists of microprogrammable standard functional modules. A single bi-directional 16-bit data bus serves to interface the CPU and sequencer logic to MTU data buffers and the IM control and data buffers. The microprogram exercises the proper data paths to perform TCU functions of bus monitor, command decode, receive, mode command operations, transmit, status word transmit and built in test.

o Bus Monitor

The RT monitors both MTUs for a command detect. When a command is detected, it is decoded and the terminal address is determined. If the terminal address belongs to the TCU, the command word is decoded. Otherwise, the TCU returns to bus monitoring.

o Command Decode

When a valid command is received, the TCU decodes the command and then performs receive, transmit, or a mode command operation depending on the contents of the command word.

o Receive Operation

The TCU receives messages from the data bus and transfers the message contents to an appropriate IM data buffer. Data messages are validated for correct parity and word count. If a message error occurs, the data buffer is not sent to the IMs and a status word is not transmitted. If the message transmission is correct, the data buffer is transferred to the IM and a status word is transmitted.

o Mode Command Operation

The TCU responds to all mode commands.

o Transmit Operation

Whenever required, the TCU transfers a status word to the MTU for transmission. The TCU monitors the validity of the transmitted data by monitoring the MTU receiver for invalid data and data parity errors. If such an error occurs, the TCU completes the current transmission and sets the appropriate error bits in the built in test word.

o Status Word Transmission

The TCU builds the status word and then commands the MTU to transmit it over the bus.

o Built In Test Word

The BIT word is maintained by the remote terminal TCU. The BIT word contains a message error field and a terminal failure field. The BIT word is shown in Figure 34.

Interface Modules

Input interface modules provide signal conditioning functions that make signals externally connected to the RT compatible with the signal interface structure defined to exist between the TCU and interface modules within the RT. Input interface modules perform the first subset of that complete set of functions necessary to convert various external signal formats into the serial-digital Manchester-encoded waveforms required for transmission of information over the data bus. Output interface modules perform the last subset of that complete set of functions necessary to convert the serial-digital Manchester-encoded waveform taken from the bus into the various signal formats required by subsystems connected externally to the remote terminal.

| MSB | | | | | | | BIT | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| POWER ON RESET | INTERFACE MODULE FAILURE | MTU 1 OUT | MTU 2 OUT | SELF TEST FAILURE | SELF TEST FAILURE | SELF TEST FAILURE | SELF TEST FAILURE | SELF TEST FAILURE | SELF TEST FAILURE | NO DATA RECEIVED | WORD COUNT HIGH | WORD COUNT LOW | DATA PARITY ERROR | INVALID DATA | INVALID COMMAND |

Figure 34 BIT Word Format and Failure Codes

o Interface Module Types

Different types of IMs exist to fulfill various requirements as follows:

(1) to interface a combination of existing air vehicle subsystems with their varied signal interface formats; (2) to interface other DAIS core elements with their standard digital interface; and (3) to allow the transition from present air vehicle subsystem interfaces to the new standard digital interface to which future air vehicle subsystems will be designed. This transition is to occur by the substitution of IMs and system reprogramming.

o Signal Mix Configuration

Different remote terminals interface with different numbers and mixes of signals dictated by peculiarities of the equipment locations where they are utilized. Configuration of an RT to interface a particular signal mix is accomplished by mounting the proper number and type of interface modules to the remote terminal housing and by appropriate system programming of the TCU.

(6) CCU/Data Bus Interface

The CCUs are connected directly to the data bus. Information on the generator system status and remote commands to the GCU are transmitted over the bus. The status information is used by the power system processor to solve system and load management equations. A data flow diagram for the GCU is shown in Figure 35.

(7) AGCU/Data Bus Interface

The AGCU provides control and protection for the APU generator and control of the auxiliary power contactor. The AGCU interfaces the data bus through a power system RT. Only the auxiliary power contactor position and APU generator load condition data is transmitted on the data bus. No control data is transmitted to the AGCU over the data bus. AGCU control signals are hardwired. The AGCU can operate independently of the data bus. A data flow diagram for the AGCU is shown in Figure 36.

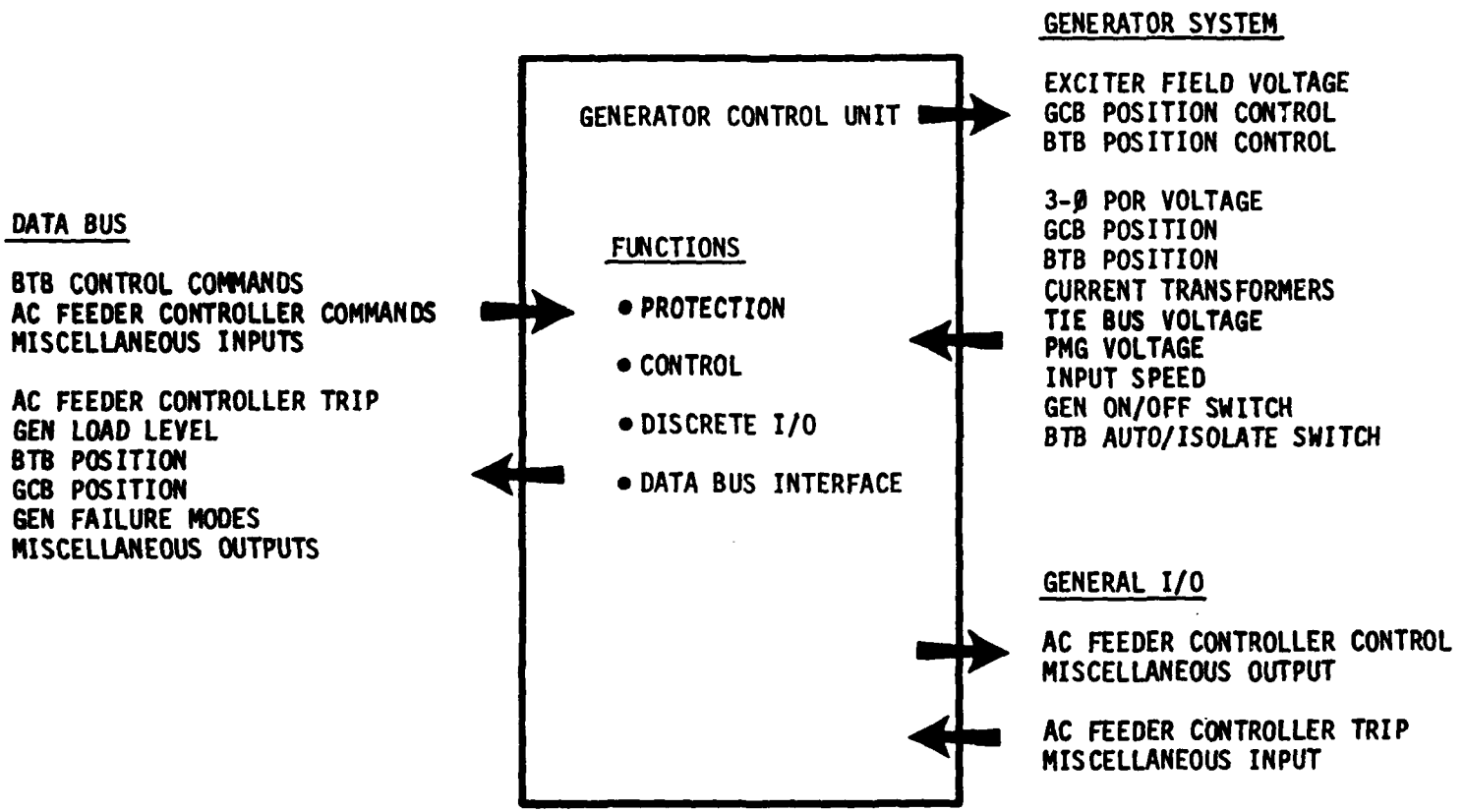



Figure 35 GCU Interfaces and Data Flow

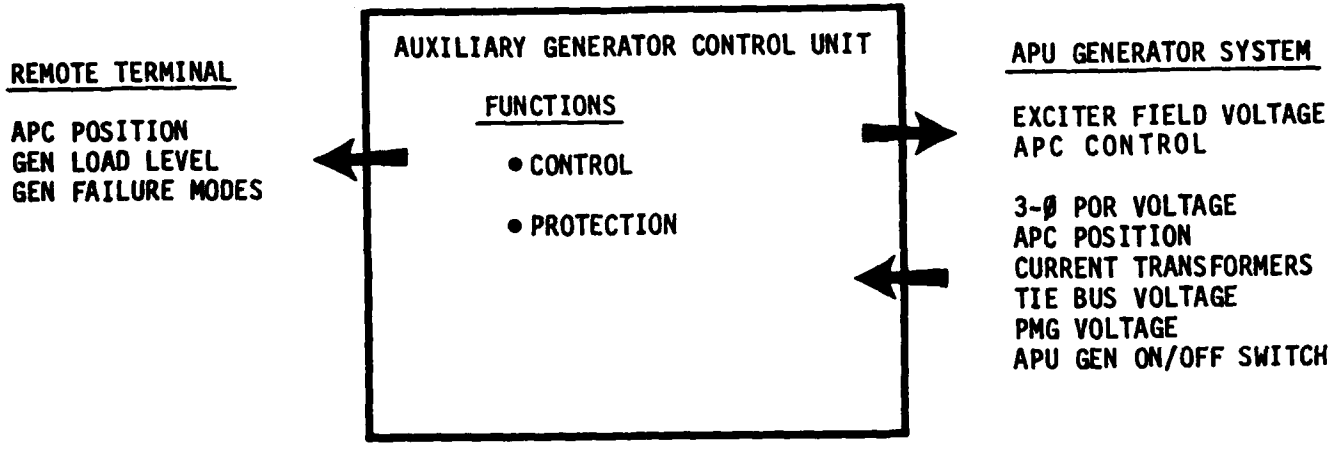



Figure 36 AGCU Interfaces and Data Flow

(8) EPCU/Data Bus Interface

The EPCU will control the external power contactor. The EPCU will also monitor the quality of the external power and will trip or inhibit the closure of the external power contactor if the limits of power quality are exceeded. The EPCU interfaces the data bus through a power system RT. External power contactor position and a "power ready" are transmitted to the PSP from the EPCU. The power system processor can send the EPCU an external power contactor trip signal over the bus. The external power ON/OFF switch is hardwired to the EPCU. A data flow diagram for the EPCU is shown in Figure 37.

3. Reliability, Maintainability, and Safety

The PSP and the ELMCs provide the capability for load management and automatic bus switching which is necessary to achieve a high mission completion success probability. The AAES architecture provides dual redundant electrical power and distribution for mission essential subsystems. In addition, three DC power sources are provided for the flight control system. For additional backup to provide the minimum flight control capability, battery power is provided. The dual MIL-STD-1553B data bus with its inherent high reliability provides a redundant link between the control logic, the electrical loads, and the power generation and distribution system. As the design progresses to greater levels of detail, reliability and safety analyses will be performed to assure that no single failure points exist that can cause loss of mission or loss of aircraft. Also, quantitative predictions will be made to determine compliance to the MIL-F-9490B flight controls mission completion success probability and aircraft safety requirements.

The PSP and other avionics computers on the MIL-STD-1553B data bus provide exceptional capability for condition monitoring, fault detection, isolation and repair verification of the AAES. This coupled with accessibility considerations during the detail packaging design will assure a high degree of maintainability.

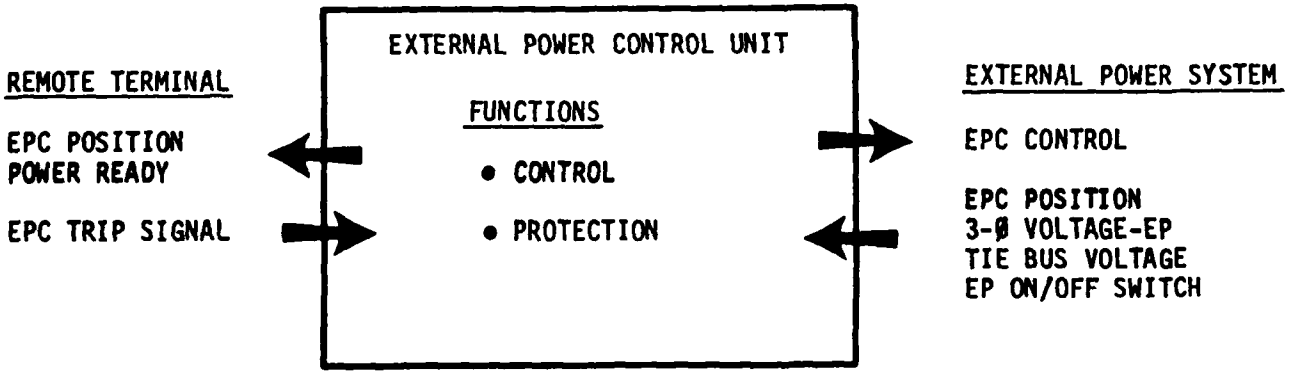



Figure 37 EPCU Interfaces and Data Flow

SECTION IV

# LABORATORY SIMULATOR PRELIMINARY DESIGN

The laboratory simulator uses existing DAIS components to simulate an integrated avionics and power control information system. The purpose of the simulator is to verify the feasibility of an integrated DAIS architecture supporting both power and avionics management functions on a single DAIS 1553B multiplexed data bus for a variety of aircraft mission equipment load complements. The laboratory simulator provides different levels of bus loading so that it can monitor performance characteristics for different combinations of bus loading and PSP equation processing response times. In addition, the simulator simulates several different operational modes for the integrated power and avionics information system including startup, load management level change, electrical power generation system configuration change, and fault isolation.

## 1. Configuration

A block diagram showing the proposed laboratory simulator configuration is presented in Figure 38.

## 2. Hardware

The laboratory simulator includes the following hardware elements:

- Bus Monitor
- System Test Console
- Generator Drive Stands
- Load Banks
- Generator Control Unit (GCU)
- Electrical Load Management Center (ELMC)
- AN/AYK-15A Computer
- Console with CRT
- Avionics Simulator and Bus Controller
- Remote Terminal
- Actual Avionics Loads

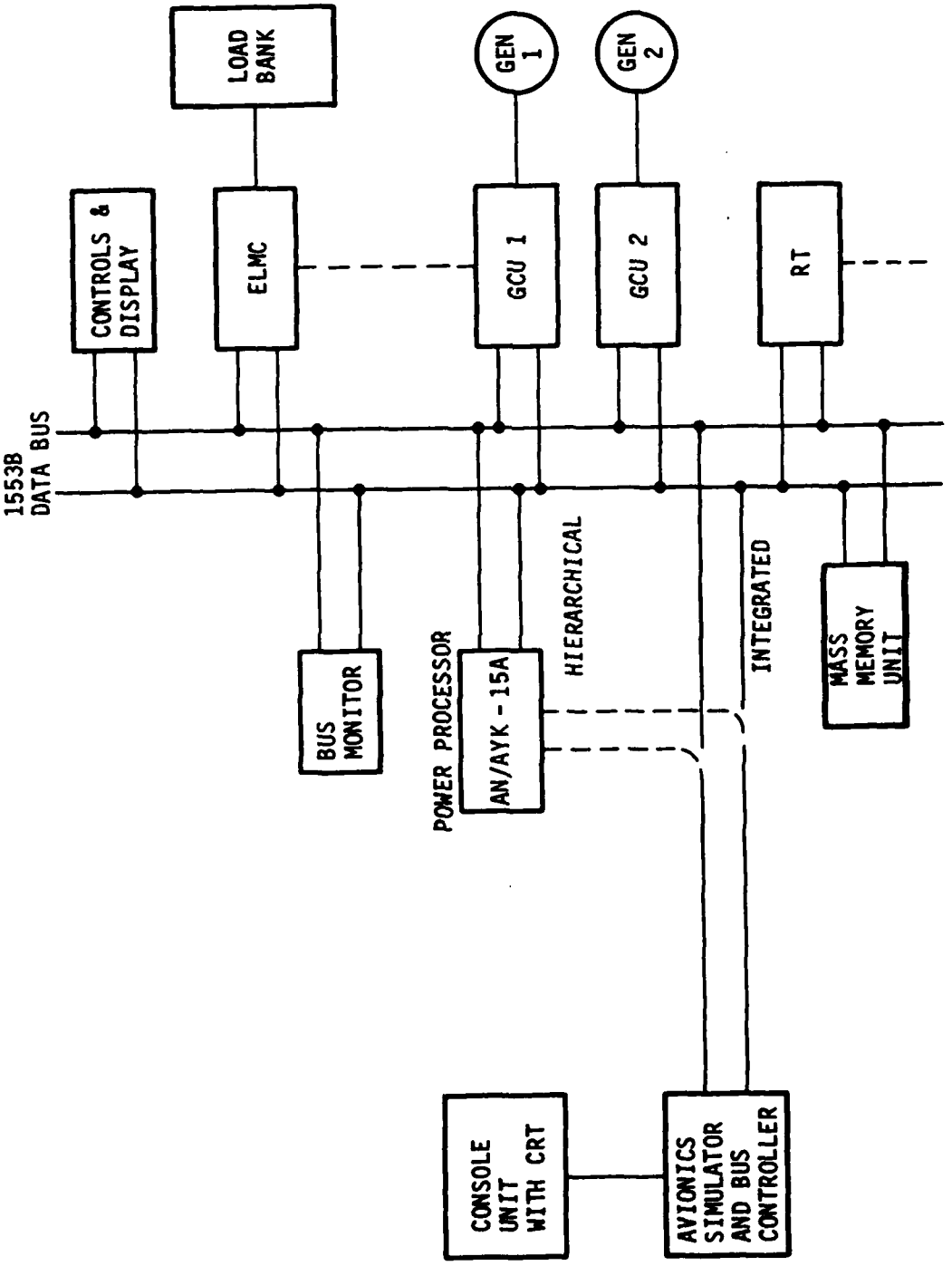



Figure 38 Laboratory Simulator Block Diagram

Requirements associated with each of the simulator elements are described below.

a. Bus Monitor

The bus monitor receives records of all bus messages and stores these messages for possible later analysis.

b. System Test Console

The system test console allows the simulator operator to perform a variety of functions in order to test and verify the integrated avionics and electrical control information system. Among capabilities provided are the ability to cause open and short circuit conditions in the electrical power distribution system and in the SSPCs. The system test console also provides display of power system status messages, display of all overload trip data, and display of addresses of all failed terminals. In addition, the system test console allows an operator to generate override commands for inhibiting automatic load management configuration, electrical system startup and shutdown messages, and to generate system stress tests by changing bus loading and bus response times.

c. Generator Stand

The generator stand provides the capability to test two generators on line simultaneously.

d. Load Bank

The load bank provides the capability to load the system SSPCs. All loads interface to ELMC SSPCs or to AC distribution buses directly via electro-mechanical power controllers.

e. Generator Control Unit

The GCU contains a remote terminal that provides the interface between the DAIS 1553B data bus and the electrical power generator. The GCU also provides

the interface with the 1553B bus for the main AC bus control and status data. For the laboratory simulator, it may not be necessary to develop special GCUs with RTs. Instead, existing GCUs could be modified to interface to DAIS RTs.

f. Electrical Load Management Center

The ELMC performs several different functions as part of the laboratory simulator. These functions include control and monitoring of SSPCs and collecting SSPC TRIP status. In addition, the ELMC receives power requests from the 1553B data bus and controls and monitors AC and DC power bus interfaces to the SSPCs.

g. AN/AYK-15A Computer

The AN/AYK-15A computer, containing 128K 16 bit words of memory performs power system management functions in the laboratory simulator.

h. Console with CRT

The laboratory simulator console and CRT provide an operator interface to the power system processor executive software for activation and suspension of tasks. The console and CRT also provide for operator examination of power system processor memory contents.

i. Avionics Simulator and Bus Controller

The avionics simulator and bus controller performs several different functions as part of the laboratory simulator. Functions performed by the avionics simulator and bus controller include control of all 1553B data bus traffic, generation of bus messages containing errors for failure simulation, and simulation of avionics bus loading traffic. The avionics simulator and bus controller also provide the interface between the PSP and the system test console and determine when failure by hardware devices attached to the 1553B data bus occurs.

j. Remote Terminal

The laboratory simulator remote terminal inputs and outputs discrete and analog data from test sensors.

3. Software

The laboratory simulator requires software to be developed for the bus controller and the avionics simulator only. The power system processor and any ERTs that are used in the laboratory simulator will use software that is developed for use on the aircraft. The bus monitor software will perform functions necessary to monitor and analyze messages that are transmitted on the DAIS 1553B data bus. This software will provide snapshots and error trapping of bus messages in order to facilitate debugging, testing, and verification of electrical control system hardware and software components. The avionics simulator software will provide those functions of the avionics processor that are essential for successful operation and testing of the advanced aircraft electrical control system. These functions include control of the DAIS 1553B multiplex data bus, simulation of avionics controls data and functions to the electrical control system, loading of the data bus to simulate avionics bus traffic, and processing of avionics display data.

## SECTION V

## WORK EFFORTS FOR DETAILED DESIGN

In this section work efforts required to complete the detailed design scheduled for Phase II of this program are described.

### 1. Avionics Processor

The avionics processor is a DAIS AN/AYK-15A computer. Existing avionics executive and application software is used. Software modifications will be minimal. These modifications are required for data transfer between the avionics processor and the power system processor. Modifications are also required to accommodate the controls and displays requirements of the electrical system since the avionics processor controls the existing DAIS control terminals.

The following work efforts are required for the avionics processor:

- o Identify data transfer requirements between the avionics system and electrical control system
- o Develop software requirements for electrical control system use of DAIS controls and displays

### 2. Power System Processor

The power system processor (PSP) is a DAIS AN/AYK-15A computer. The DAIS executive software will be modified for the PSP. The PSP application software is new and a specification for this software will be developed. The PSP application software covers almost all facets of the electrical system operation and thus requires several areas of detailed development. These areas are listed below:

- o Load management operation
- o Define inputs to load management algorithm
- o Define power request equations
- o Define priority management operation
- o Develop built-in-test procedure and requirements for the electrical system

PSP Executive Software

A standard DAIS single processor synchronous executive, specification #SA 221308 must be modified so that it provides an interface to the 1553B data bus, but does not perform bus control functions.

3. ELMC

The ELMC is a new item. Both hardware and software must be developed. Hardware development focuses on two areas, the SSPCs and the ERT. The software development also focuses on two areas, the ERT executive and the ERT application software.

a. ELMC Hardware

(1) SSPCs

The SSPCs will be packaged on printed circuit cards. Input/output connections to the SSPCs will be made through edge connectors. The work efforts to accomplish this design are:

- o Determine thermal requirement
- o Determine card size
- o Standardize on number of SSPCs per card based on current rating
- o Determine SSPC control interface based on wiring and circuitry constraints

(2) ERT

The ERT hardware development is straightforward. The data developed during the preliminary design must be translated into detailed requirements specifications. An analysis of the impact on packaging and interfacing 100 SSPCs with a 4-wire system and a 2-wire system will be made. Based on this analysis a decision on the interface will be made.

b. ERT Software

(1) ERT Executive Software

The ERT executive software must be developed. This executive will be patterned after the DAIS single processor synchronous executive, as in specification SA 221308. This executive must be modified so that it does not perform bus control functions.

(2) ERT Application Software

The ERT application software covers the control and monitoring of the SSPCs, control and monitoring of the power distribution center, and processing of general I/O to be defined. The following work efforts will be required:

- o Define aircraft load complement
- o Define ELMC discrete I/O and analog inputs
- o Define load control equations
- o Define procedures for load management priority level changes

4. Remote Terminals

DAIS RTs are used in the system. The I/O requirements for the RTs must be defined so that the proper interface modules can be specified for the RTs and any new design requirements for the interface modules can be identified and designed.

5. GCU

The GCUs for the AAES are presently designed with a built-in data bus interface. This represents a new design for GCUs. A detailed design will be performed for the GCU in Phase II. To accomplish the design, the following efforts will be required:

- o Identify generators to be used in the simulator
- o Define time delays required for the GCU protective functions
- o Define GCU discrete and analog I/O

6. Controls and Displays

Existing DAIS controls and displays unit will be used by the system. In addition, a control panel for the electrical system will be developed. This panel will supplement the DAIS unit. In Phase II the following efforts will be required:

- o Identify data to be displayed on DAIS C & D
- o Identify functions for the control panel

SECTION VI

# CONCLUSIONS AND RECOMMENDATIONS

## 1. Results and Conclusions

Task 3 of Phase I of the Advanced Aircraft Electrical System Control Technology Demonstrator Program consisted of preparing a preliminary design of the electrical power system with an integrated electrical/avionics data bus architecture. Drafts were prepared of Part I specifications of the overall system and the major component hardware and software. The preliminary performance requirements for the Power System Processor, Electrical Load Management Center, and Electrical Remote Terminals were defined. The software for the PSP and ERT are divided into the Executive and Applications Software. Both the PSP and ERT will use the DAIS Single Processor Synchronous Executive (DAIS Part I Specification SA 221308) with minor modifications and will not include the bus control functions. In the integrated architecture design the bus control function will reside in the Avionics Processor.

Outlines of the Part I specifications of the System Test Console and the Advanced Electrical Power System (AEPS) Simulator have also been prepared. All draft specifications are included in a separate document, as is a draft outline of the Initial Demonstration Plan.

Preliminary design of the ELMC indicates there may be problems with packaging 100 SSPCs in the ELMC. The area of concern is the amount of wiring required to interface the SSPCs to the ERT and the loads. Further examination is planned in this area. The results may be a change in the SSPC interface method or a decrease in the number of SSPCs per ELMC. If the latter determination is made, further study of the impact of this change on the data bus loading and PSP processing will be required. Also during the design of the ERT it was discovered that a 16 bit microprocessor capable of executing the MIL-STD-1750 instruction set was not available. A Jovial compiler is not available for the Z8002 microprocessor presently selected for the ERT.

Preliminary design studies for the laboratory simulator indicate that the bus monitor and the avionics simulator/bus controller functions can be performed by off-the-shelf hardware boxes at a cost of approximately $20K each. Two such boxes would be needed. It will be necessary to build the ELMC/ERT, and to provide a power system processor, DAIS RT, and a generator control unit in addition to a load bank and operator console in order to successfully implement the laboratory simulator.

A preliminary hazard analysis (PHA) of the system was conducted and is documented separately. This PHA indicates that none of the major component failures will be of a catastrophic or critical category, and thus the program can move from the preliminary to detailed design phase without major reorientation.

All aspects of the design indicate that the basic integrated architecture for avionics/power system control is feasible and should continue into the next phase. The design philosophy selected segregates the avionics data bus traffic and power system data bus traffic by utilizing separate avionics and power system processors and allows considerable flexibility by minimizing, if not eliminating, the impact of changes in one from the other. An added benefit of this design philosophy is the capability of transitioning the design from an integrated to a hierarchical data bus architecture. For this transition the PSP would need to be enhanced to include the bus controller functions and interbus processing functions. The interbus processing capability for the PSP is not planned to be developed in this program, however.

## 2. Recommendations

Since the preliminary design of the integrated avionics/electrical power system control architecture does indicate that such a system is feasible, it is recommended that the program be allowed to proceed into the detailed design phase. Specific activities to be conducted in the tasks for the aircraft electrical system design and the design of support hardware and software are defined in the Design and Development Plan for Phase II which is documented separately.

Consideration should be given to expanding the scope of Phase II by the addition of a third task to develop the hardware modifications and software necessary for the Interbus Processor. This additional task will enhance the capability of the design to be rapidly reconfigured from an integrated bus to a hierarchical bus architecture and make the system compatible with aircraft which require separate data buses for avionics and electrical system controls.

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